

# Compal Confidential

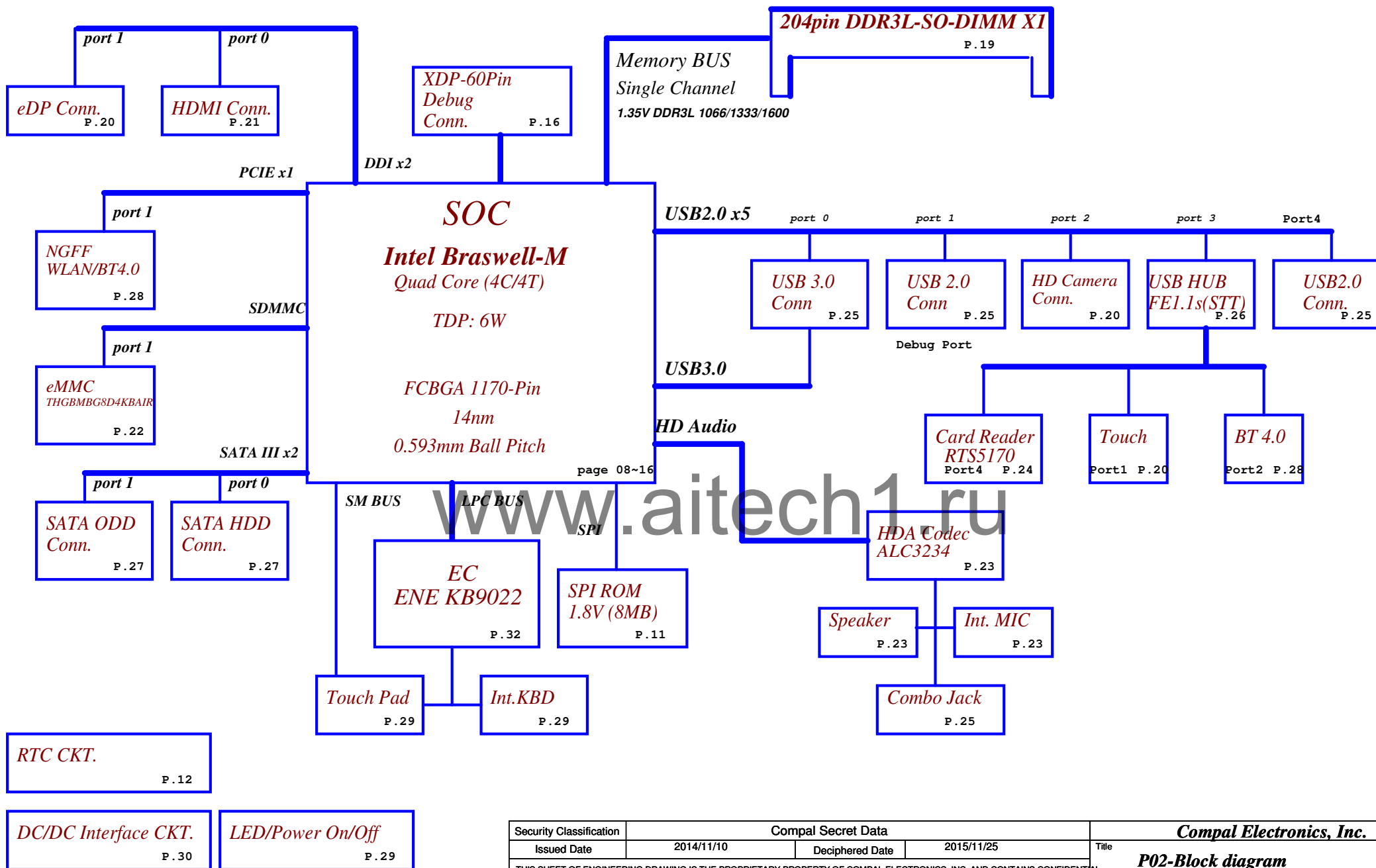
## Schematic Document

Intel Braswell M  
UMA  
www.aitech1.ru

2015-6-09      Rev: 1.0

ZZZ PCB®  
PCB 1EE LA-C571P REV1 M/B 2  
DA6001DX010

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		LA-C571P		Date	Tuesday, June 16, 2015
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## Voltage Rails

Power Plane	Description	S0	S3	S4/S5
VIN	19V Adapter power supply	ON	ON	ON
BATT+	12V Battery power supply	ON	ON	ON
B+	AC or battery power rail for power circuit. (19V/12V)	ON	ON	ON
+RTCVCC	RTC Battery Power	ON	ON	ON
+1.05VALW	+1.05v Always power rail	ON	ON	ON
+1.24VALW	+1.24v Always power rail	ON	ON	ON
+1.8VALW	+1.8v Always power rail	ON	ON	ON
+3VALW	+3.3v Always power rail	ON	ON	ON
+3V_SOC	+3V_SOC Always power rail	ON	ON	ON
+5VALW	+5.0v Always power rail	ON	ON	ON
+1.35V	+1.35V power rail for DDR3L	ON	ON	OFF
+VCC_CORE	Core voltage for SOC	ON	OFF	OFF
+VGG_CORE	GFX voltage for SOC	ON	OFF	OFF
+0.675VS	+0.675V power rail for DDR3L Terminator	ON	OFF	OFF
+1.15VALW	+1.15VALW system power rail	ON	OFF	OFF
+1.35VS	+1.35v system power rail	ON	OFF	OFF
+1.5VS	+1.5v system power rail	ON	OFF	OFF
+1.8VS	+1.8v system power rail	ON	OFF	OFF
+3VS	+3.3v system power rail	ON	OFF	OFF
+5VS	+5.0v system power rail	ON	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

## Board ID / SKU ID Table for AD channel

Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID_min	VAD_BID_typ	VAD_BID_max	EC_AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xEE
19	NC	3.000V	3.300V	3.300V	0xEF - 0xFF

## BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0

## BOM Option Table

Item	BOM Structure
Unpop	@
Connector	CONN@
XDP (Debug Port)	XDP@
EMC requirement	EMI@
EMC requirement unpop	NEMI@
LPC18	LPC18@
LPC33	LPC33@
Rvs. RF requirement	RF@
ESD requirement	ESD@
XDP (Debug Port) unpop	NXDP@
ESD requirement unpop	NESD@
For JUMP	JP@
For PCB	PCB@
For CPU	SOC@ SOC1@
SATA re-Driver	601@
Test Point	TP@
SATA re-Driver unpop	N601@

## 43 level BOM table

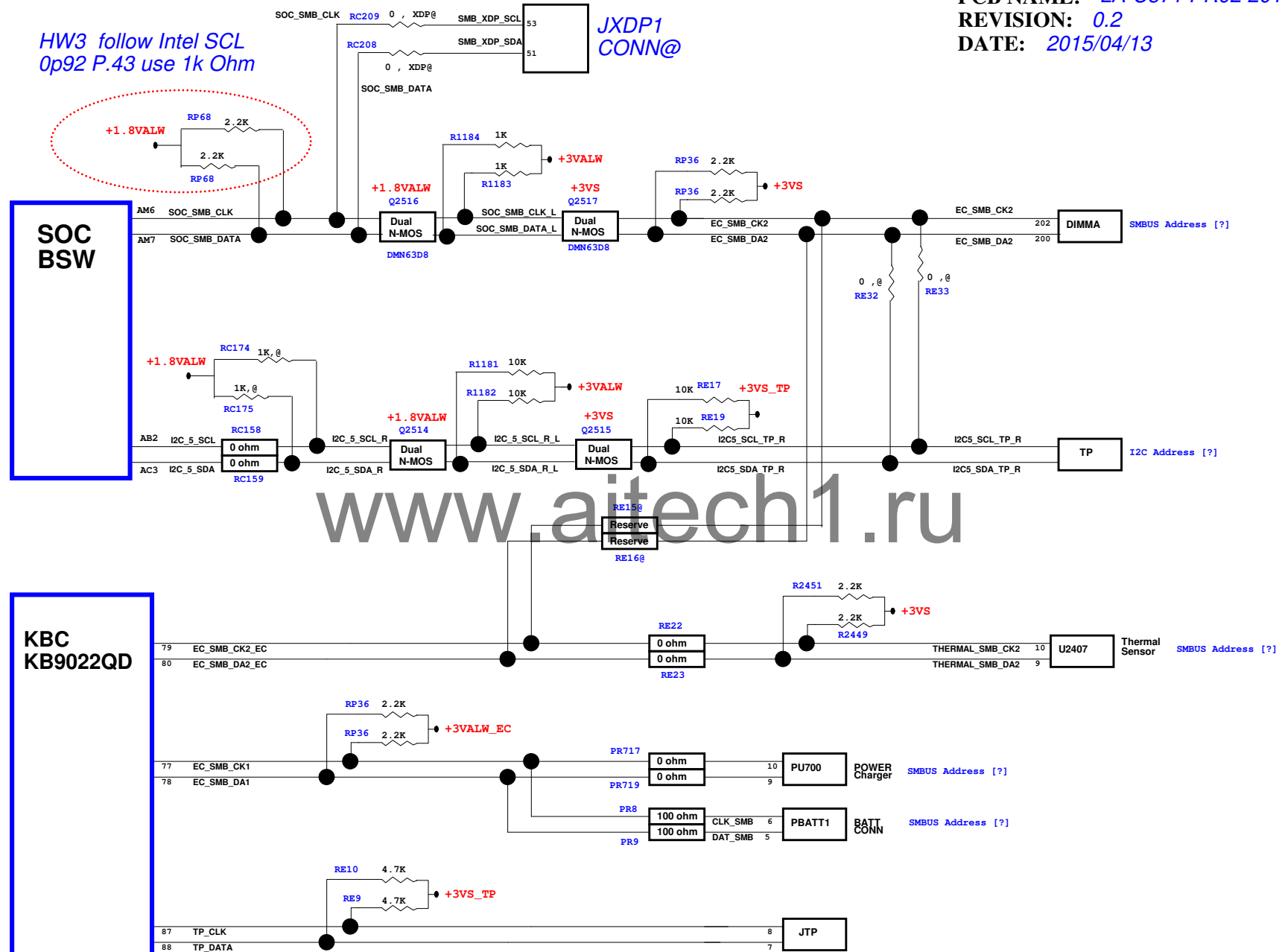
43 Level	Description	BOM Structure
4319Y031L01	MB AC571 AAL14 BSW U PEN HDMI	EMI@/ESD@/XDP@/LPC33@/PCB@/ODD@/SOC@/601@/N601@/PARADE@
4319Y031L02	MB AC571 AAL14 BSW U CEL HDMI	EMI@/ESD@/XDP@/LPC33@/PCB@/ODD@/SOC1@/601@/N601@/PARADE@

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MODEL NAME: *SMBus Block Diagram*  
PCB NAME: *LA-C571 PR02 2015/03/27*  
REVISION: *0.2*  
DATE: *2015/04/13*

*HW3 follow Intel SCL  
Op92 P.43 use 1k Ohm*

*JXDP1  
CONN@*

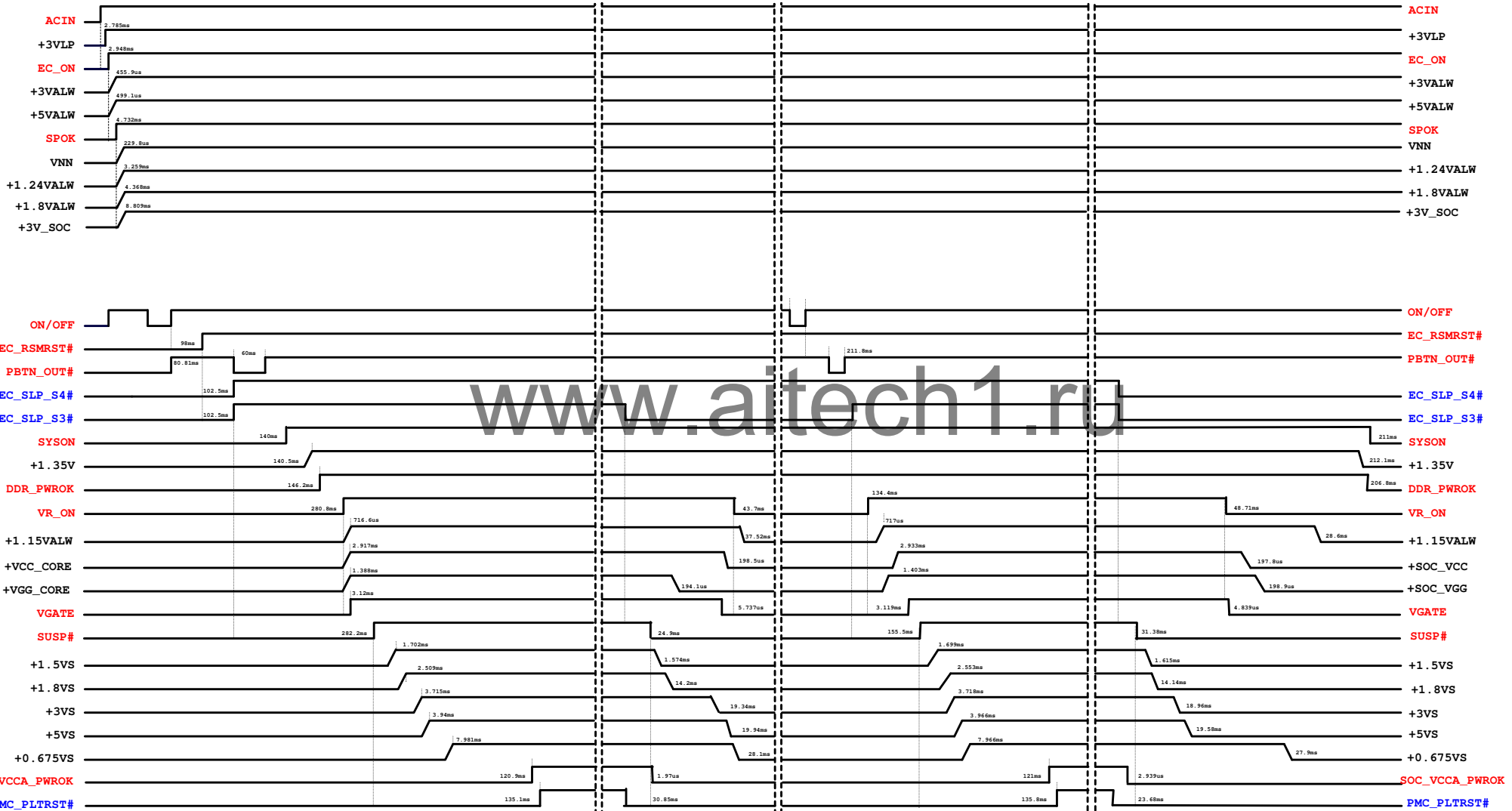


S5-&gt;S0

S0-&gt;S3

S3-&gt;S0

S0-&gt;S5



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**DATE:** 2015/04/13



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				Issued	7 of 8

Main Func = CPU

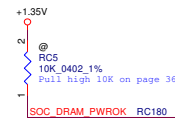
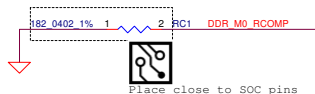
UC1  
SOC@

S IC A31 FH806501715906 QJMS C0 1.6G  
Part Number = SA00008U62L

UC1  
SOC@

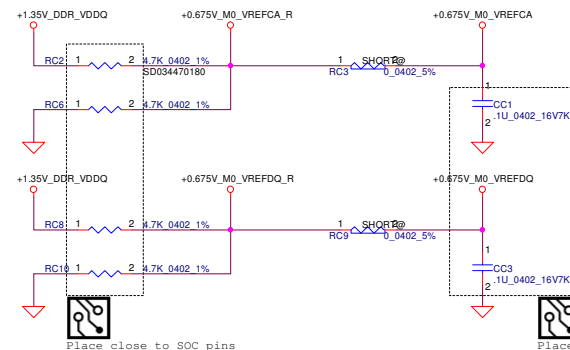
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Part Number = SA00008U52L

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Power Name and Connection Check OK

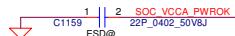
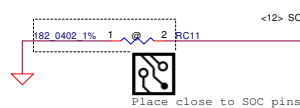
8 mils minimum for maximum of 300 mils in breakout area



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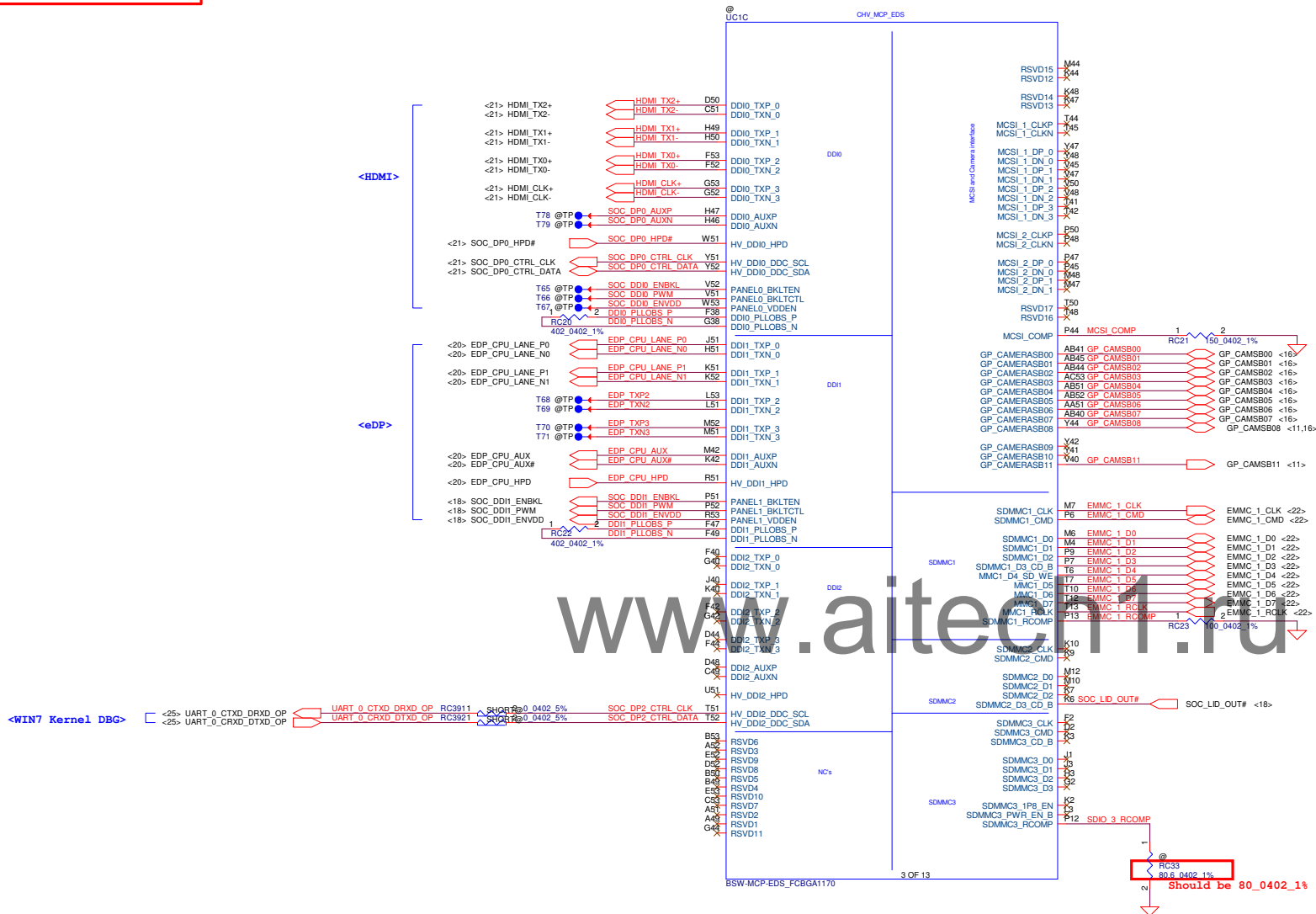
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CHV_MCP_EDS		
UC1B	DDR1	
BD5	DDR3_M1_MA_15	BD21
BD7	DDR3_M1_MA_14	BD26
BF10	DDR3_M1_MA_13	BD25
BB5	DDR3_M1_MA_12	BD26
BJ8	DDR3_M1_MA_11	BD22
BE2	DDR3_M1_MA_10	BD20
BD10	DDR3_M1_MA_9	BD25
BE8	DDR3_M1_MA_8	BD21
BB8	DDR3_M1_MA_7	BD26
BH8	DDR3_M1_MA_6	BD24
BD12	DDR3_M1_MA_5	BD20
BH2	DDR3_M1_MA_4	BD24
BJ2	DDR3_M1_MA_3	BD20
BC12	DDR3_M1_MA_2	BD24
BE2	DDR3_M1_MA_1	BD20
BF2	DDR3_M1_MA_0	BD20
AY18	DDR3_M1_BS_2	AV22
BH2	DDR3_M1_BS_1	AV20
BC9	DDR3_M1_BS_0	BD18
BA18	DDR3_M1_CASB	BF18
BH10	DDR3_M1_RASB	AV22
AU18	DDR3_M1_WEB	AV20
AY18	DDR3_M1_CSB_1	BA18
BD18	DDR3_M1_CSB_0	BC18
BF18	DDR3_M1_CK_1	BH18
AY12	DDR3_M1_CKB_1	BH18
BD14	DDR3_M1_CKB_0	BJ13
BF10	DDR3_M1_CK_0	BH12
BB10	DDR3_M1_CKB_0	BJ17
AT24	DDR3_M1_CKE_0	BG17
AU24	RSVD1	BG11
AV18	RSVD2	BG12
BA18	DDR3_M1_ODT_0	BB3
AT28	DDR3_M1_ODT_1	AV11
AU28	DDR3_M1_OCAVREF	BC2
BA12	DDR3_M1_ODQVREF	AV3
AY28	DDR3_M1_DRAMRSTB	BC1
BA26	DDR3_M1_VCCA_PWROK	AV2
BH24	DDR3_M1_RCOMP	BD2
BD22	DDR3_M1_RCOMP	AV12
AY18	DDR3_M1_DM_7	AP13
BG14	DDR3_M1_DM_6	AV13
BA18	DDR3_M1_DM_5	AT10
AP10	DDR3_M1_DM_4	AP14
AT8	DDR3_M1_DM_3	AT16
AP2	DDR3_M1_DM_2	AP12
BH22	DDR3_M1_DM_1	AT14
BG22	DDR3_M1_DM_0	AV9
BC22	DDR3_M1_DQS_7	AV4
AT22	DDR3_M1_DQS_6	AT4
BH12	DDR3_M1_DQS_5	AP7
BG12	DDR3_M1_DQS_4	AV4
AY2	DDR3_M1_DQS_3	AV6
AT2	DDR3_M1_DQS_2	AT7
AV2	DDR3_M1_DQS_1	AP6
AM2	DDR3_M1_DQS_0	AP3
AM2	DDR3_M1_DQS_0	AP1
AM2	DDR3_M1_DQS_0	AK2
AM2	DDR3_M1_DQS_0	AL1
AM2	DDR3_M1_DQS_0	AP3
AM2	DDR3_M1_DQS_0	AT2
AM2	DDR3_M1_DQS_0	AL3
AM2	DDR3_M1_DQS_0	AK3
AM2	DDR3_M1_DQS_0	AK3

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BSW-MCP-EDS\_FCBGA1170

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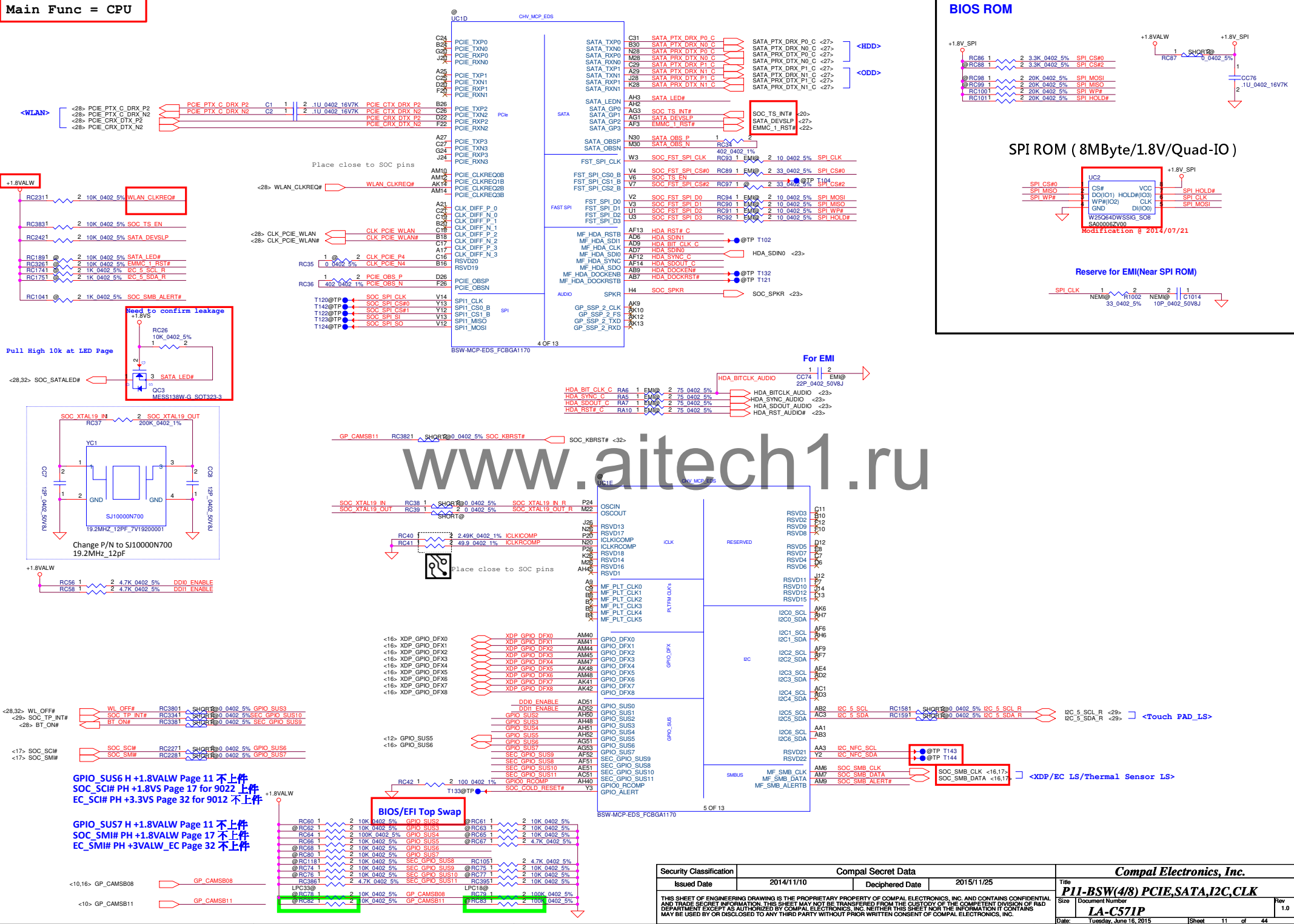
BIOS ROM

SPI ROM ( 8MByte/1.8V/Quad-IO )

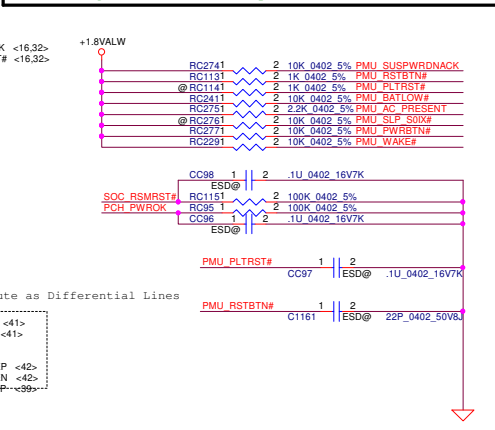
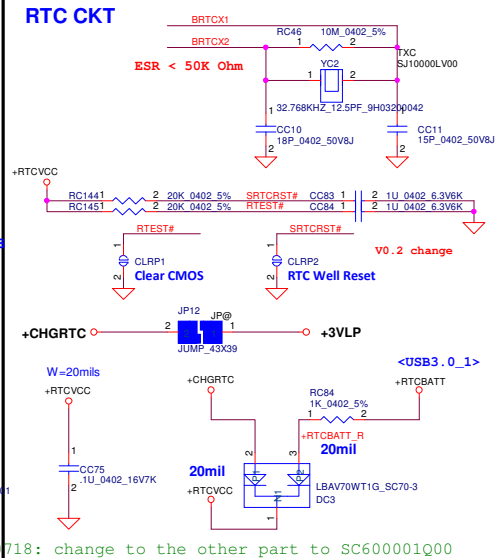
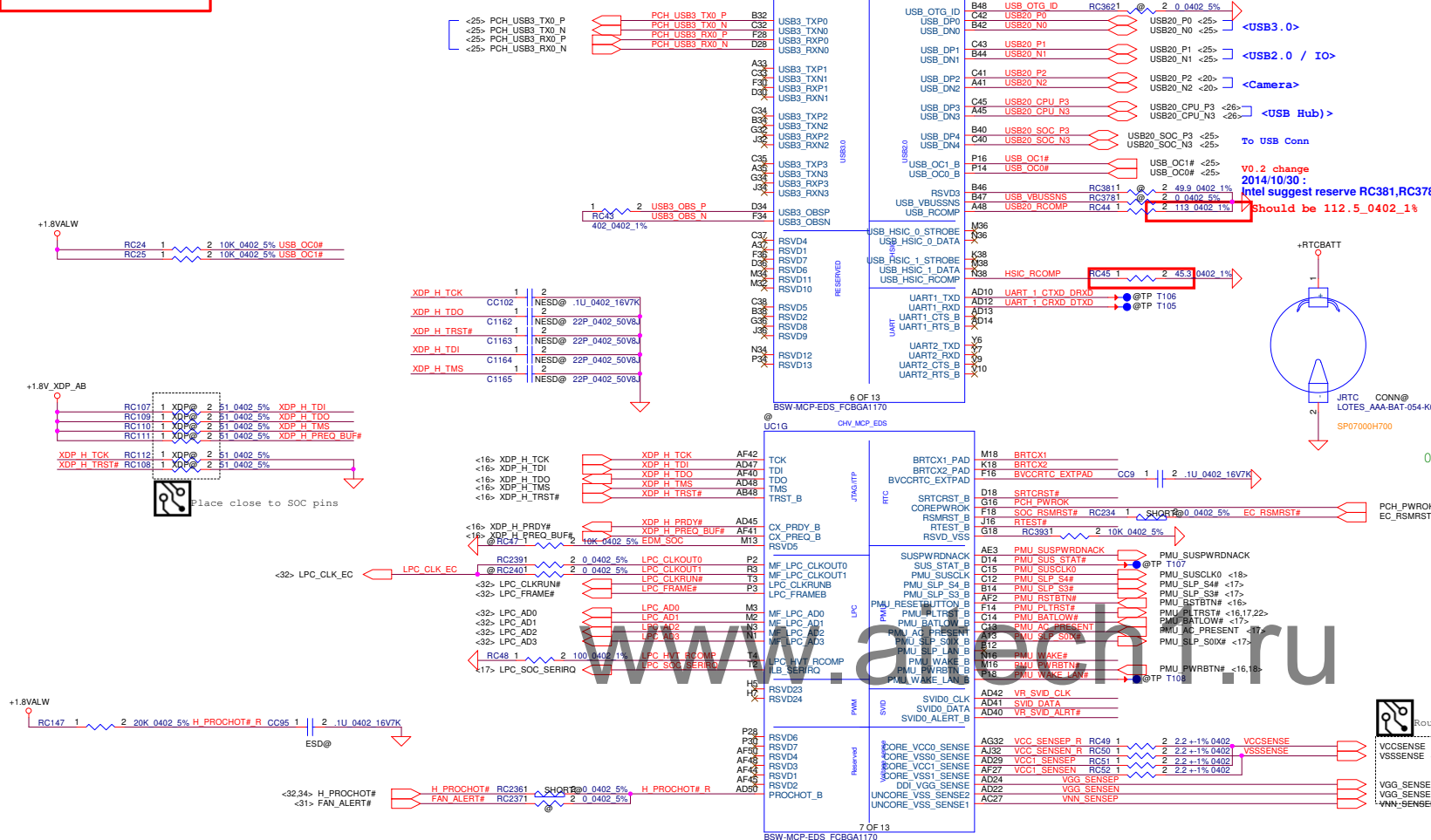
Reserve for EM(Near SPI ROM)

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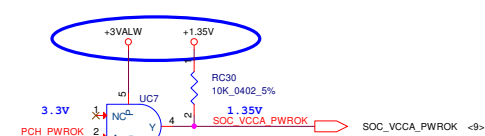
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Main Func = CPU



Hardware Strap				
Pin Name	Purpose	PU/PD	Description	Default State
GPIO_SUS0	DDI0 Detect	PD	1: DDI0 detected 0: DDI0 not detected	High
GPIO_SUS1	DDI1 Detect	PD	1: DDI1 detected 0: DDI1 not detected	High
GPIO_SUS2	A16 swap overdrive	PU	1: Normal operation 0: Change Boot Loader address	High
GPIO_SUS3	DSI Display Detect	PD	1: DSI detected 0: DSI not detected	Low
GPIO_SUS4	Boot BIOS Strap BBS	PU	1: Boot from SPI 0: Boot from LPC	High
GPIO_SUS5	Flash Descriptor Security Override	PU	1: Security enabled 0: Security disabled	High
GPIO_SUS6	DFX Boot Halt Strap, VISA Early POSM Debug Enable	PU	1: Normal operation 0: Halt boot enable	High
GPIO_SUS7	DFX Sus Debug Strap	PU	1: Normal operation 0: Sus Debug enabled	High
SEC_GPIO_SUS8	ICLK, USB2, DDI SFR Supply Select	PD	1: 1.35V supply 0: 1.25V supply	Low
SEC_GPIO_SUS9	ICLK, USB2, DDI SFR Bypass	PU	1: Bypass with 1.05V 0: No bypass	Low
SEC_GPIO_SUS10	POSM Select	PD	1: PMC 0: Fuse controller	Don't care, if GPIO_SUS6 is pulled high
GP_CAMERASB08	ICLK Xtal OSC Bypass	PD	1: Bypass 0: No bypass	Low
GP_CAMERASB09	CCU SUS RO Bypass	PD	1: Bypass 0: No bypass	Low
GP_CAMERASB11	RTC OSC Bypass	PD	1: Bypass 0: No bypass	Low



### Security Flash Descriptor

GPIO\_SUS0: 0: Override  
1: Normal Operation (internal PU)

Note: EC programming TXE\_DBG "H" for Flash BIOS

### SVID

Follow PWR Net Name -> Change to VR\_SVID\_CLK  
Note: VR\_SVID\_CLK Rs & Rpu @ power side

Note: SVID\_ALERT# Rs @ power side

Note: SVID\_DATA Rpu & Rss @ power side

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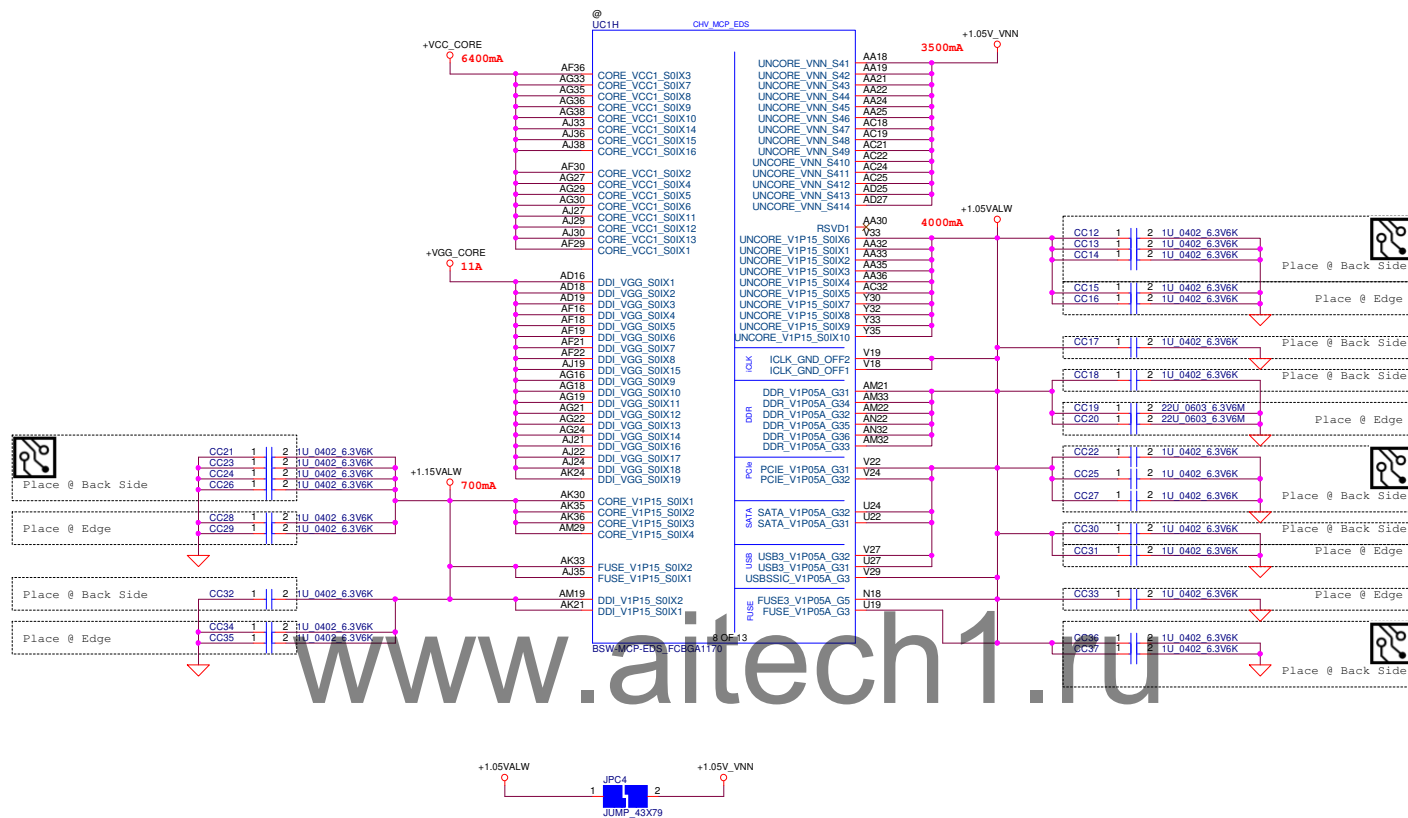
P12-BSW(5/8) USB,UART,RTC,PWM

LA-C571P

Tuesday, June 16, 2015

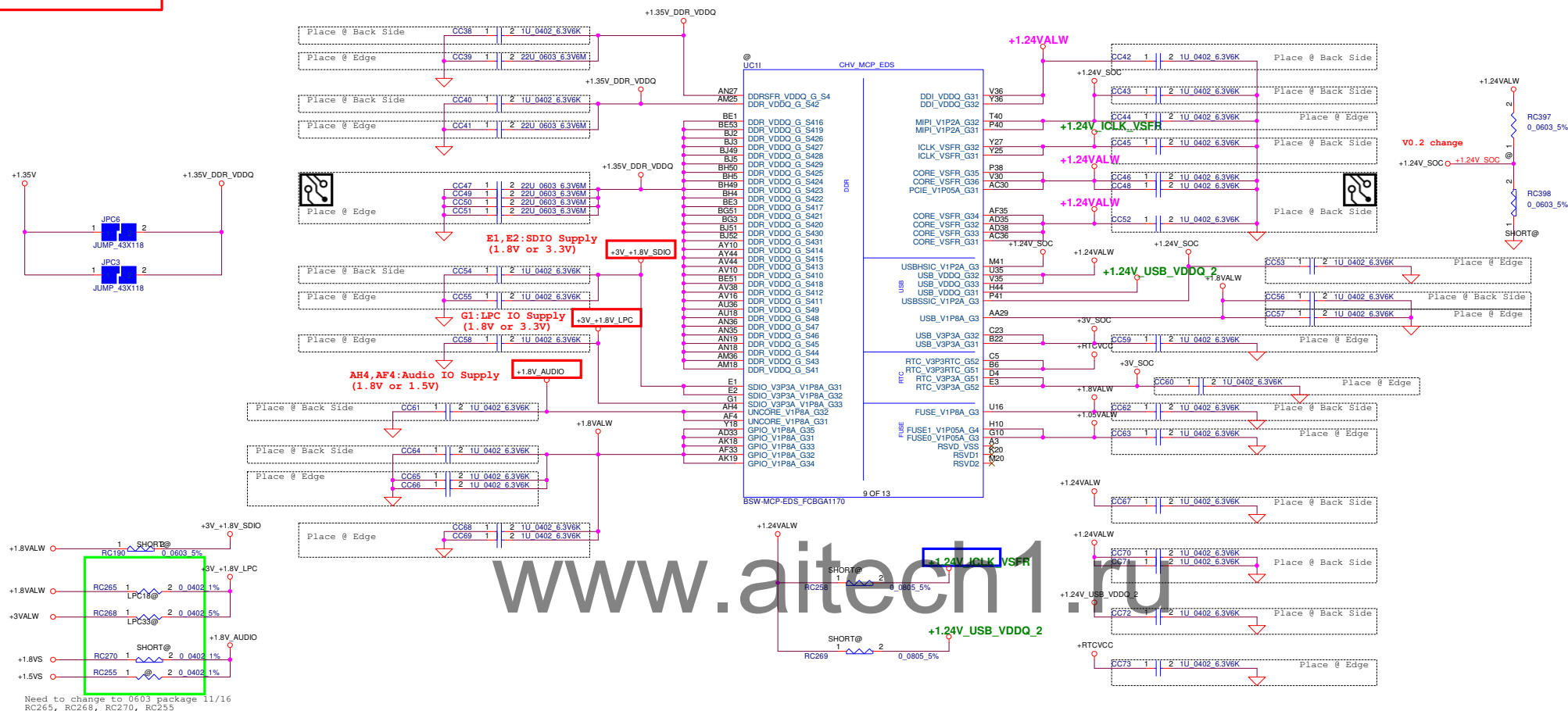
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Main Func = CPU



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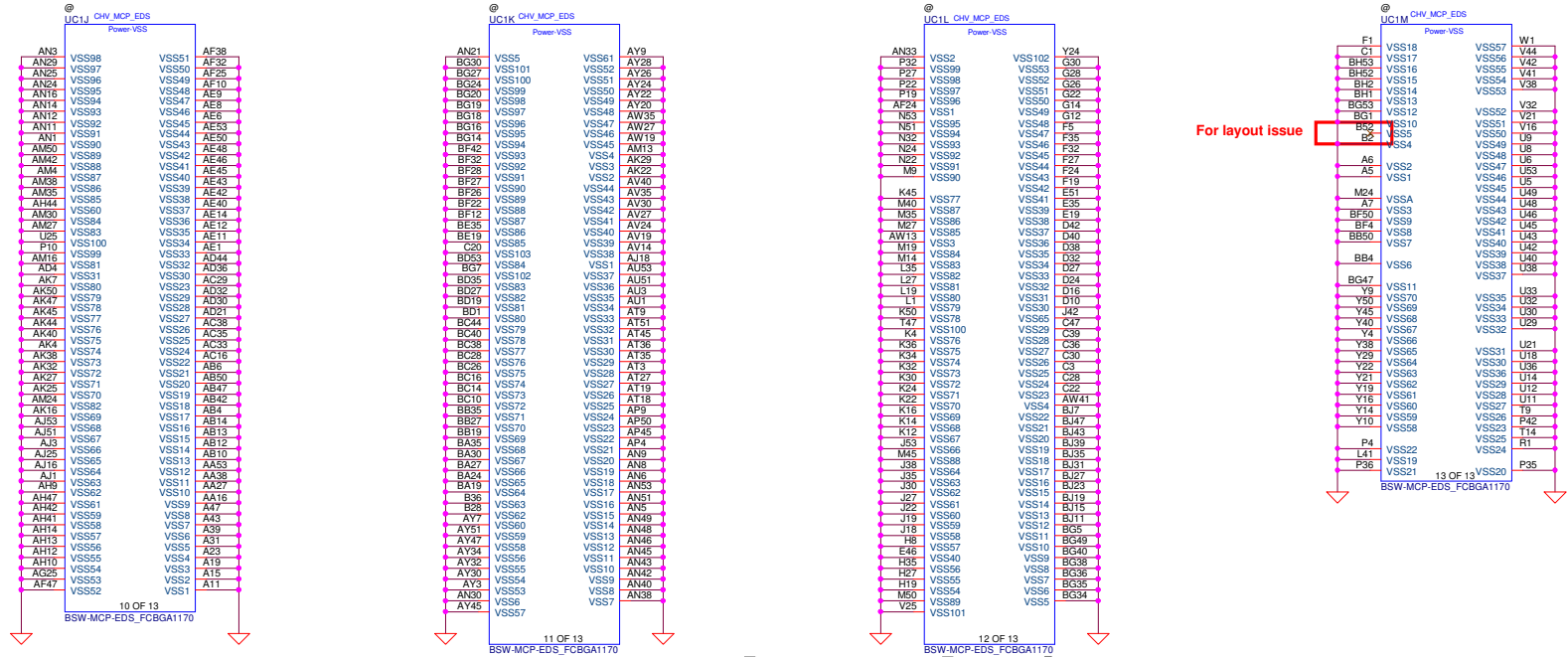


**NOTE:**  
+1.24V\_MIP1, +1.24V\_USBSSIC, +1.24V\_USBSSIC are +1.24V Only.  
[PDG Rev0p92 P.55]  
When SSIC, HSIC & CSI interface is not used, the following pins can be connected to ground:  
CSI (T40, P40), USB HSIC (M41), USB SSIC (P41).

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				Size Document Number	
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				Sheet 14 of 44	



Main Func = CPU



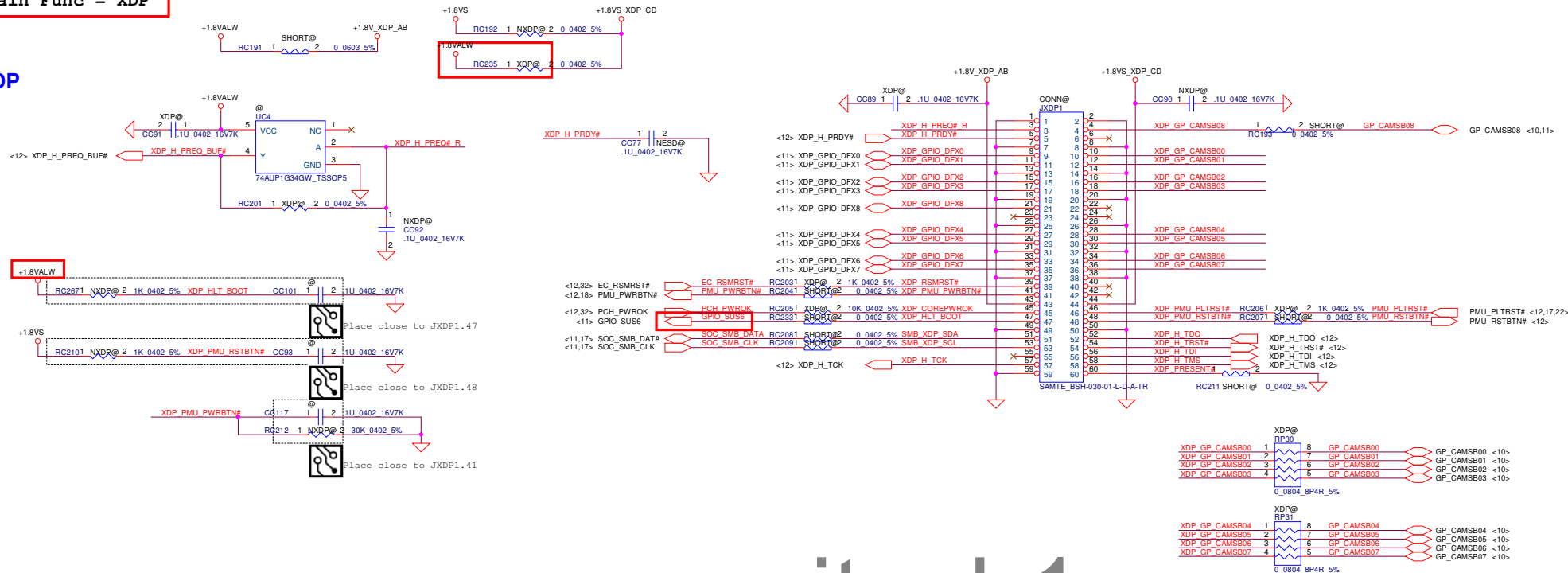
For layout issue

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				Date	LA-C571P
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				Rev	1.0

Main Func = XDP

XDP



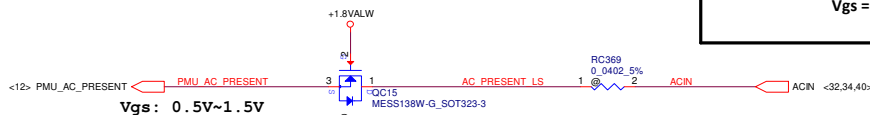
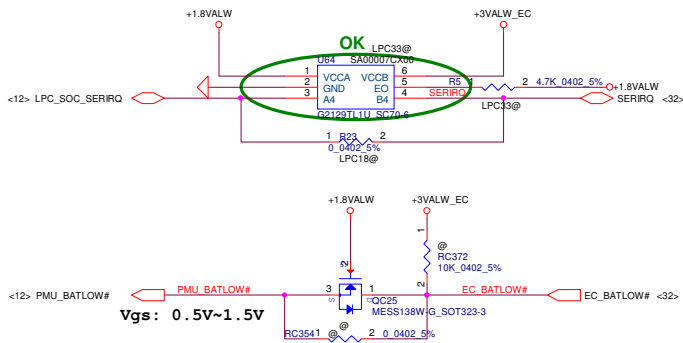
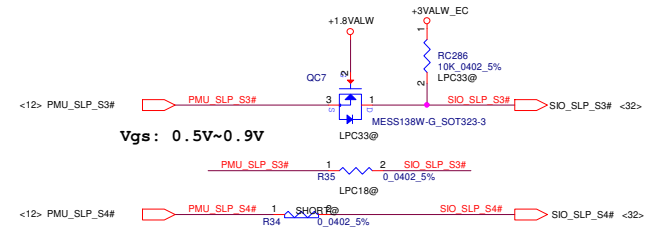
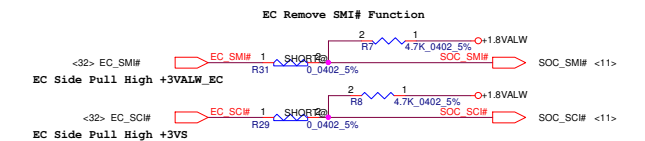
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				Date	LA-C571P
				Sheet	16 of 44

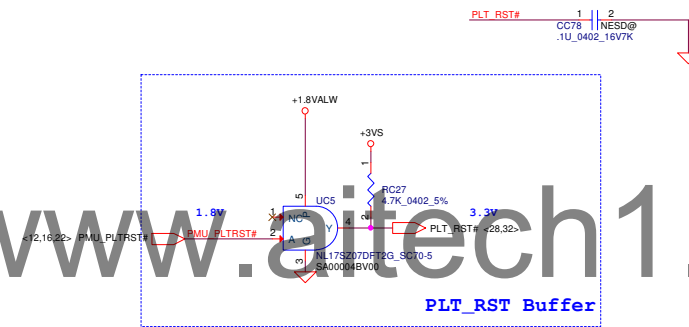
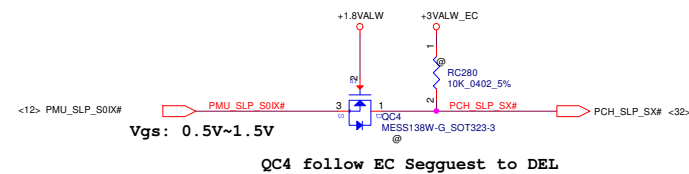


Main Func = Level Shift

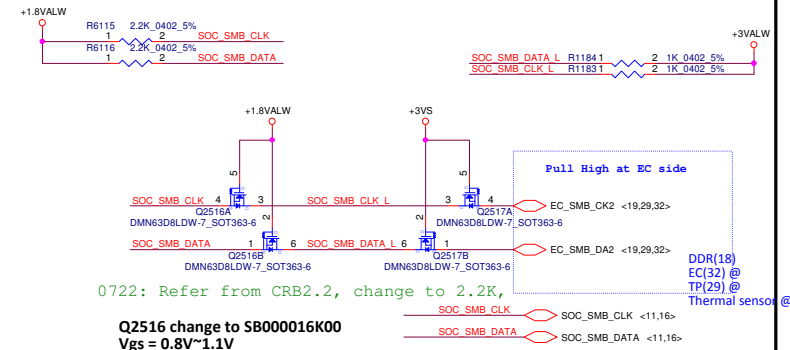
POWER ON SEQUENCE



POWER ON SEQUENCE



SMBUS  
EC/Thermal Sensor/Touch Pad



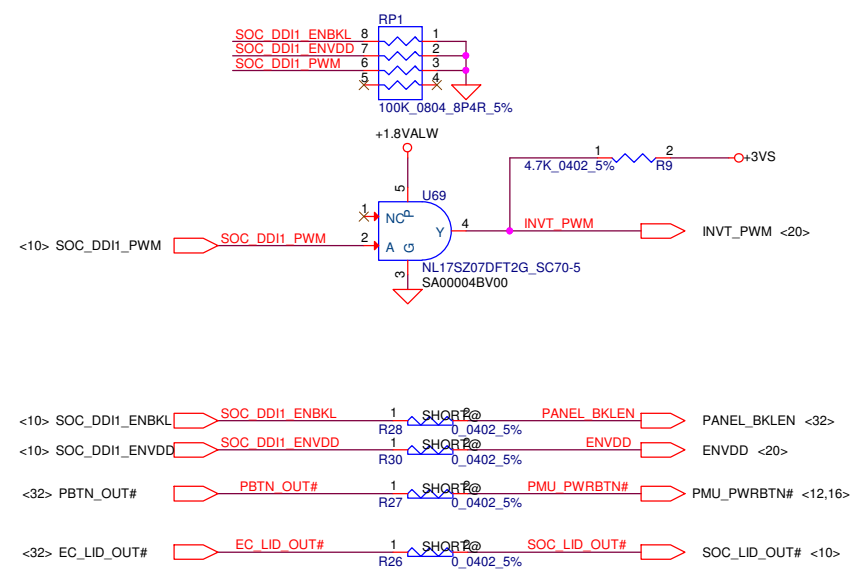
Q2516 change to SB000016K00  
Vgs = 0.8V~1.1V

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Deciphered Date	2015/11/25
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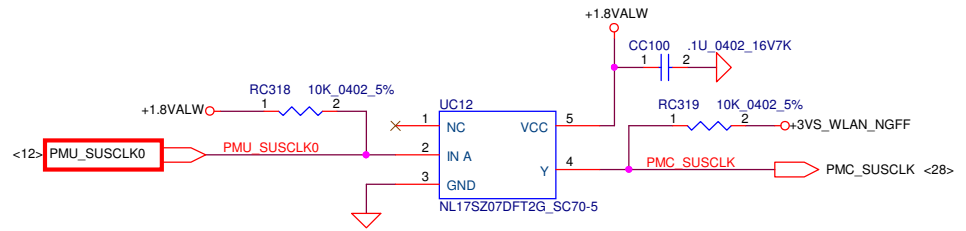
Compal Electronics, Inc.	
P17-Level Shift-1	
Size	Document Number
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Main Func = Level Shift

eDP Control



WLAN



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Main Func = DIMM

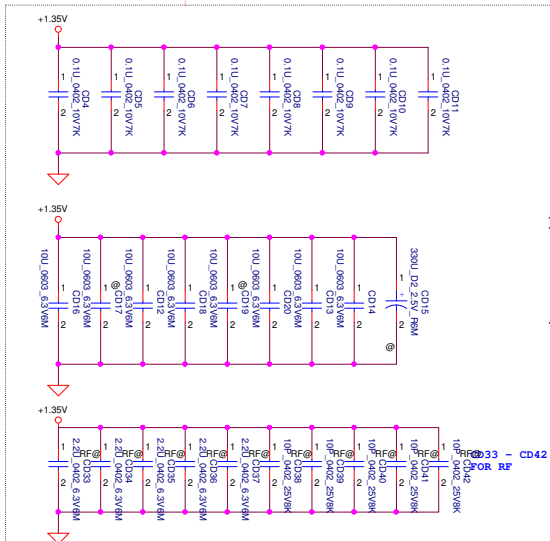
Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1  
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

<8> DDR\_M0\_DM[4,7]  
<8> DDR\_M0\_DM[0,3]  
<8> DDR\_M0\_DQS[0,7]  
<8> DDR\_M0\_DQS[0,7]  
<8> DDR\_M0\_D[0,3]  
<8> DDR\_M0\_D[32,63]  
<8> DDR\_M0\_MA[0,15]

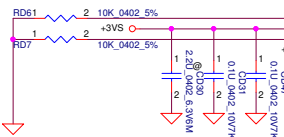
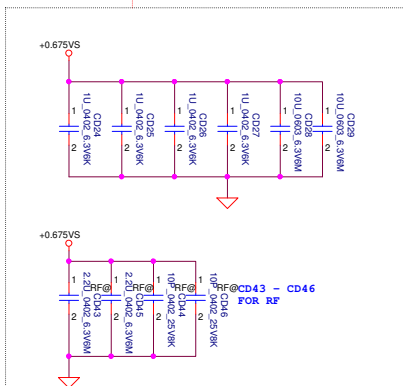
All VREF traces should have 10 mil trace width

Layout Note:  
Place near JDIMM1

Note:  
Check voltage tolerance of VREF\_DQ at the DIMM socket



Layout Note:  
Place near JDIMM1.203,204

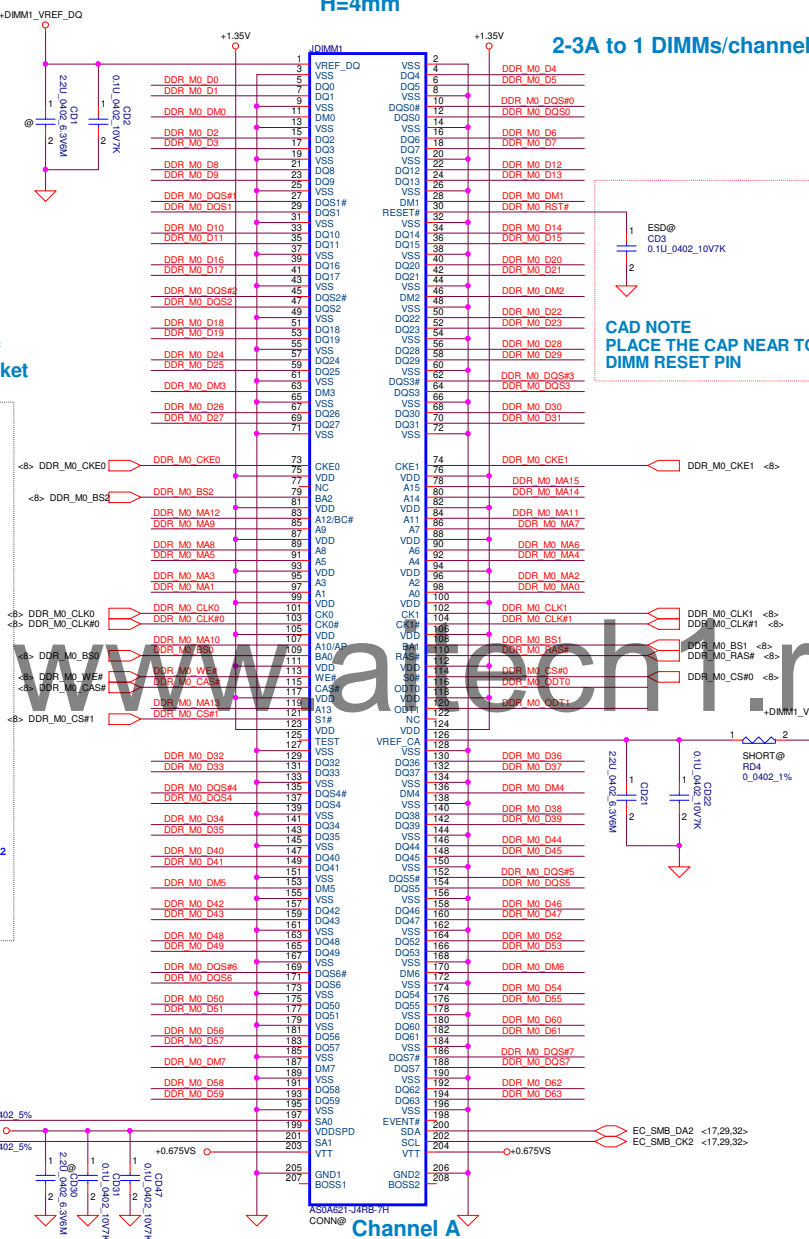


ESD solution

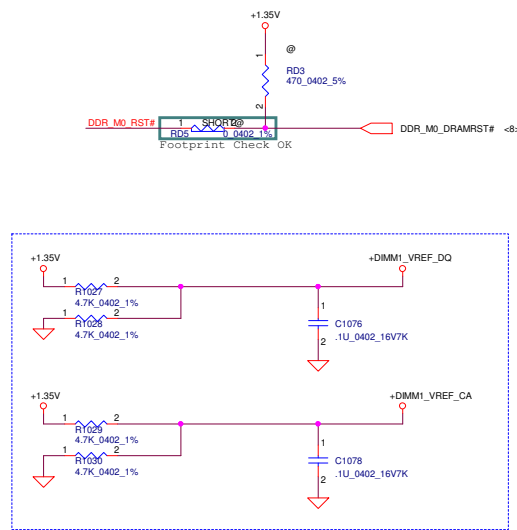
<Address: SA1:SA0=00 (A0H)>  
DIMM\_1 STD H:4mm

H=4mm

2-3A to 1 DIMMs/channel



CAD NOTE  
PLACE THE CAP NEAR TO DIMM RESET PIN

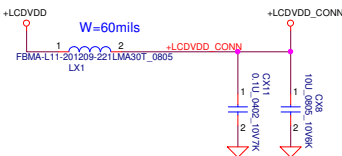
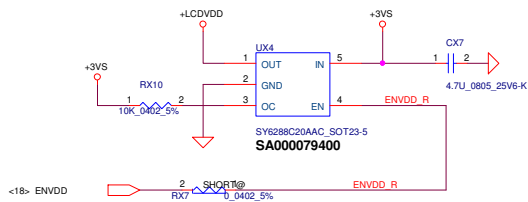


DDR\_M0\_ODT0 <8>  
DDR\_M0\_ODT1 <8>  
V0.2 change

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				LA-C571P	1.0
				Date: Tuesday, June 16, 2015	Sheet 19 of 44

Main Func = eDP

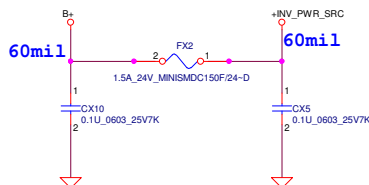
## LCD PWR CTRL



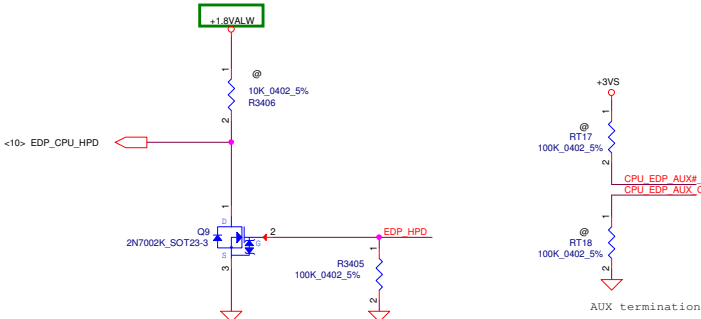
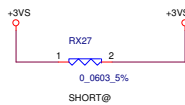
SS table

Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

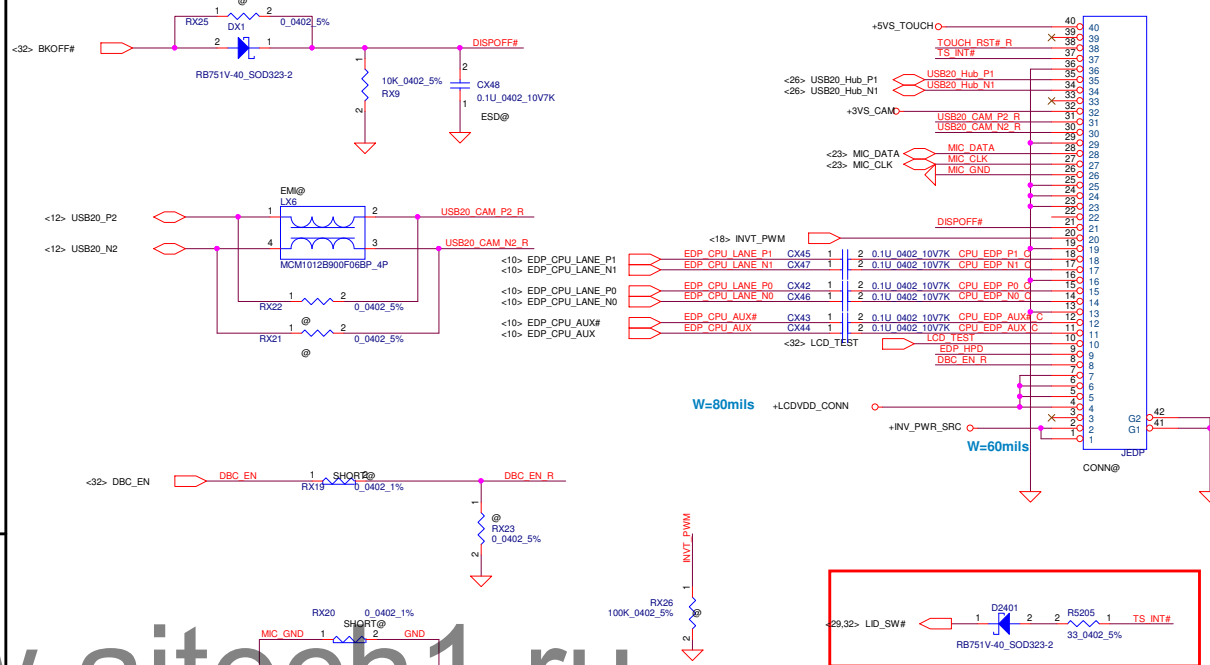
## LCD backlight PWR CTRL



## Webcam PWR CTRL

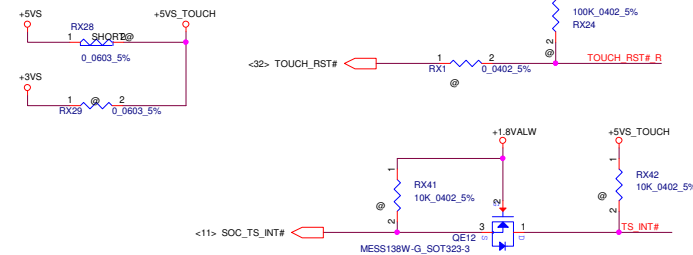


## LCD Connector



Note: Follow BDW design V0.2 change

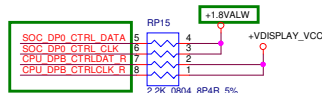
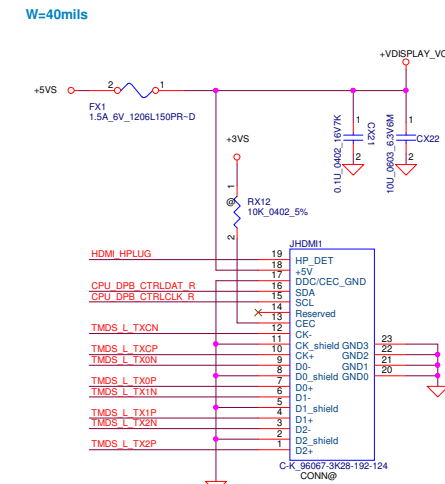
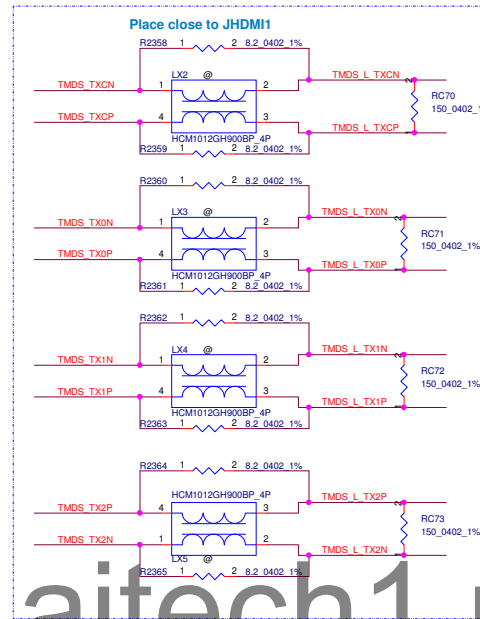
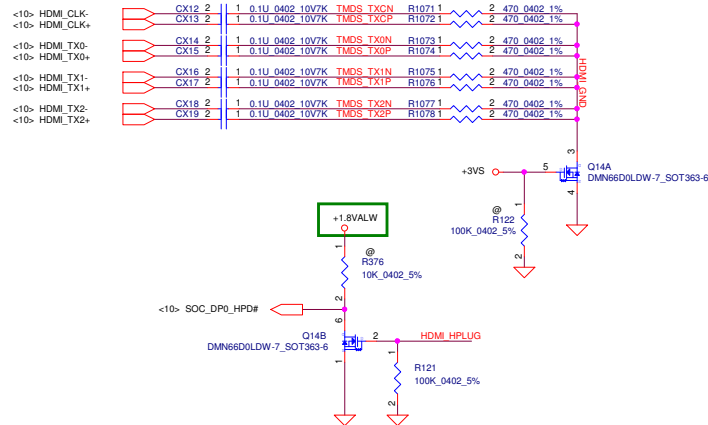
## \* Touch Screen Panel



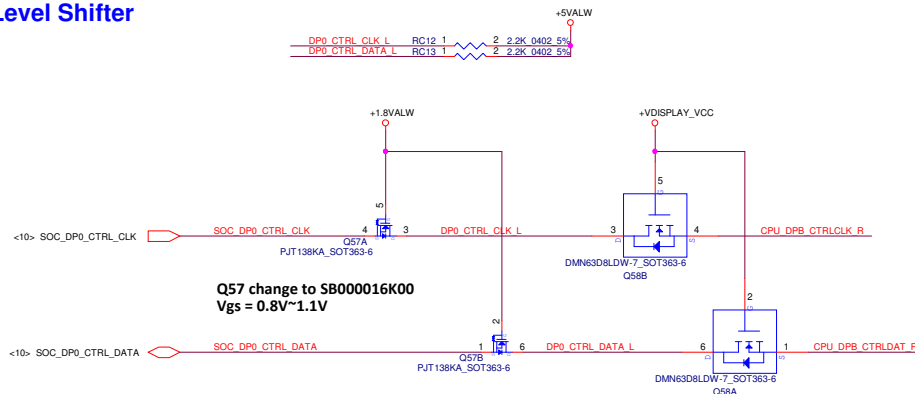
Closed to JEDP

Main Func = HDMI

Part Number	Description
RO0000002HM	HDMI W/Logo:RO0000002HM



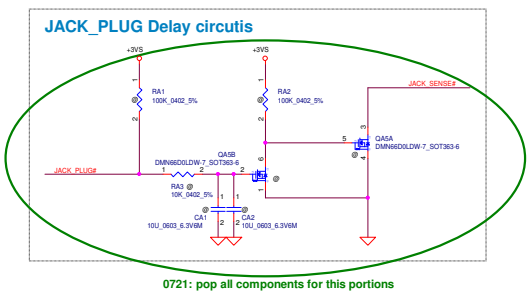
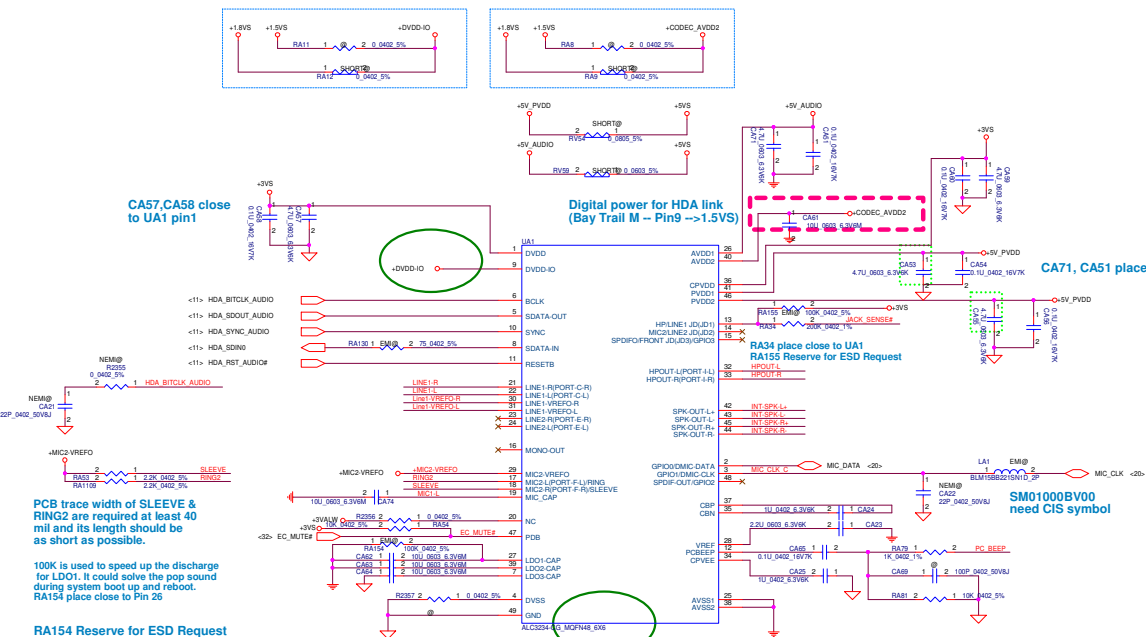
## Level Shifter



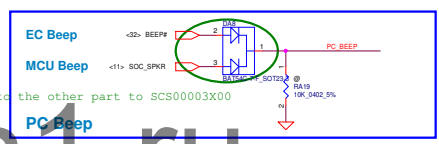
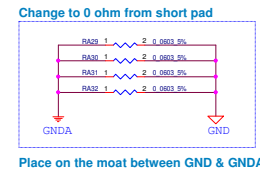
V0.2 change

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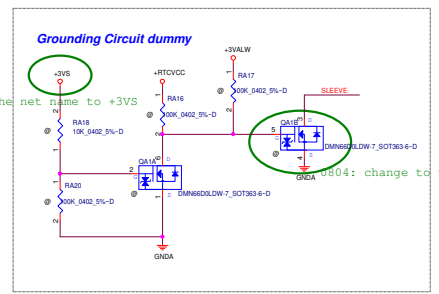
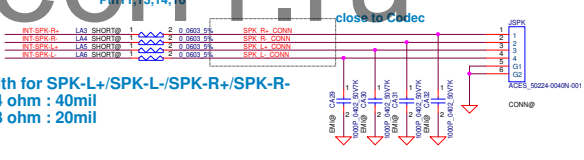
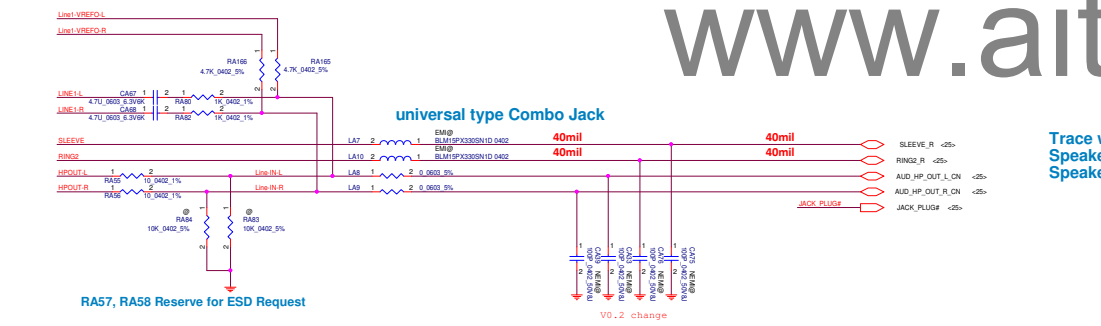




Reserve for cancel Delay circuitis

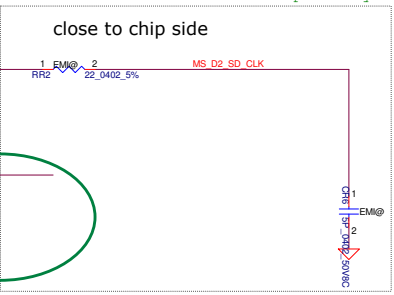
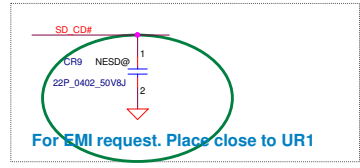
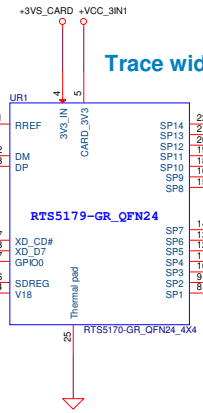
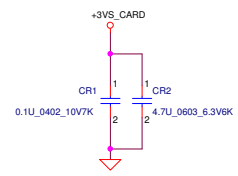
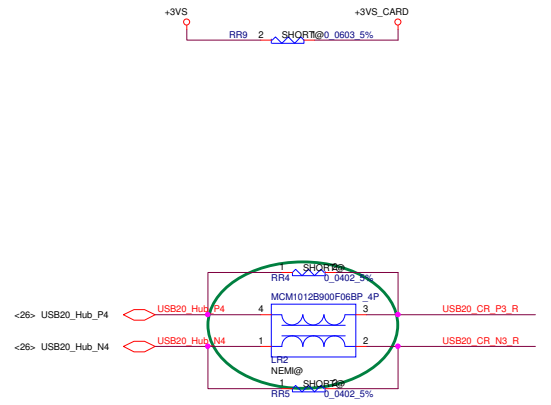


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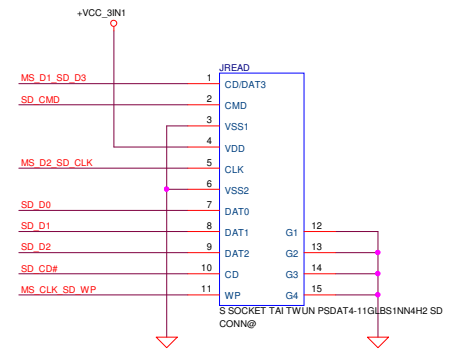
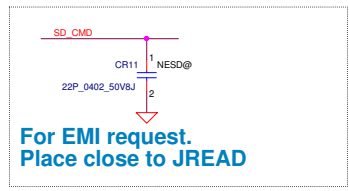
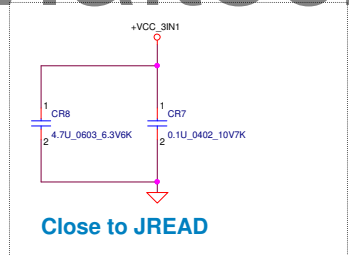


www.vinafix.com

Main Func = Card Reader



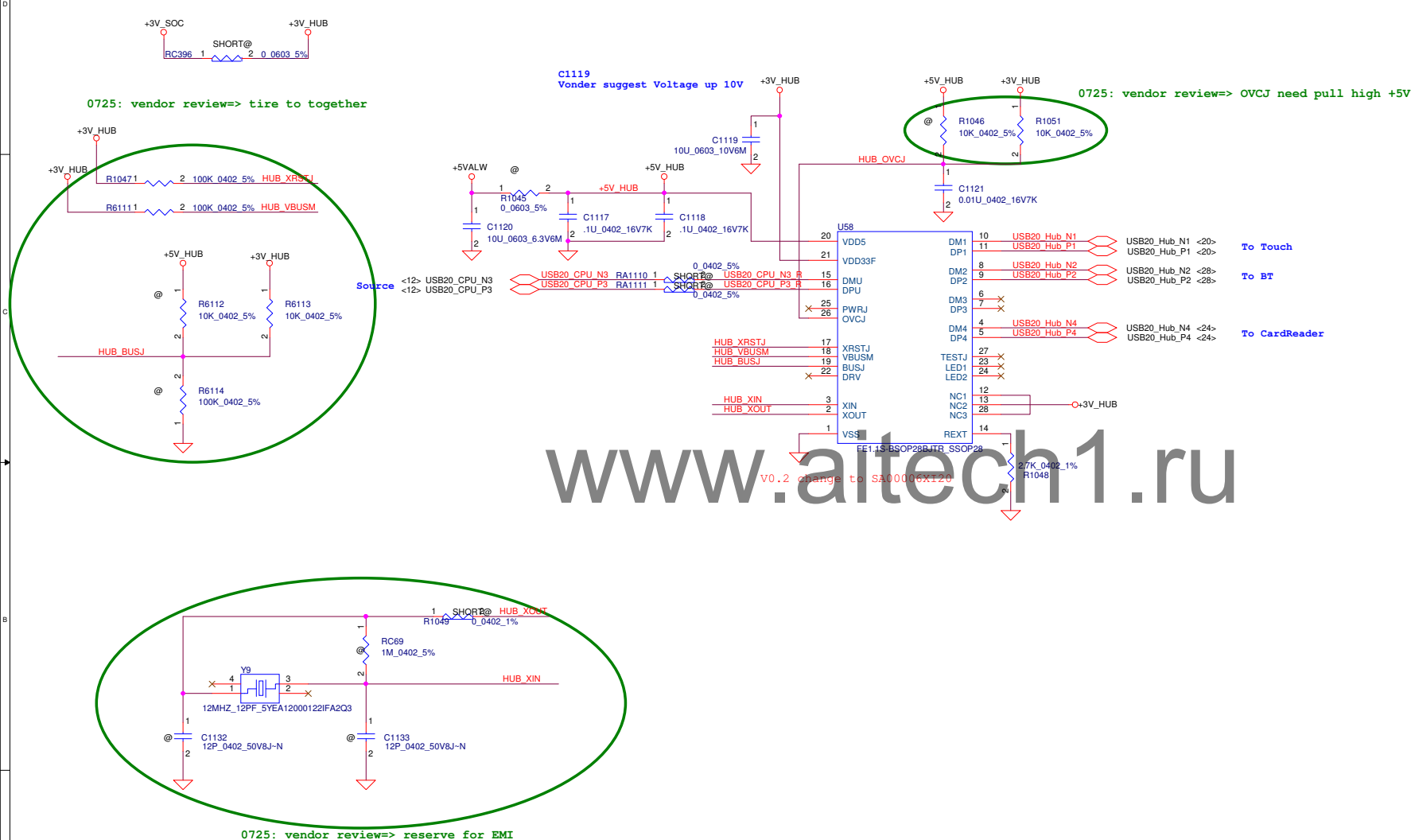
www.aitech1.ru



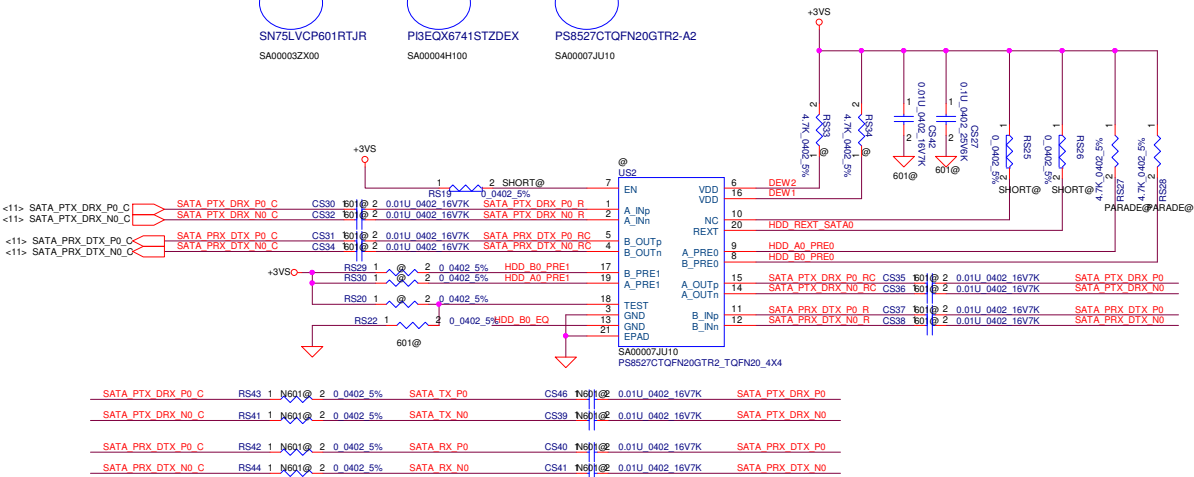




Main Func = HUB 2.0

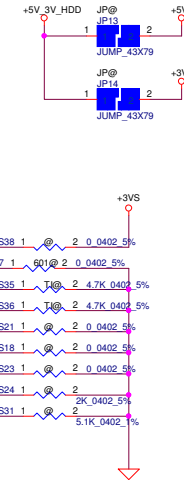


Main Func = HDD

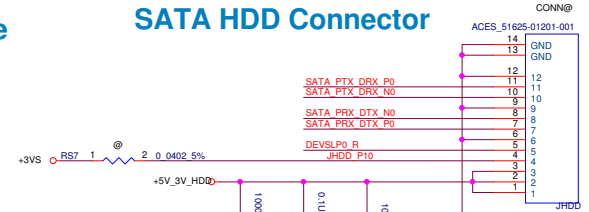


	DE	EQ
PARADE	-6dB	2.4dB
TI	-4dB	0dB

## +5V\_HDD Source

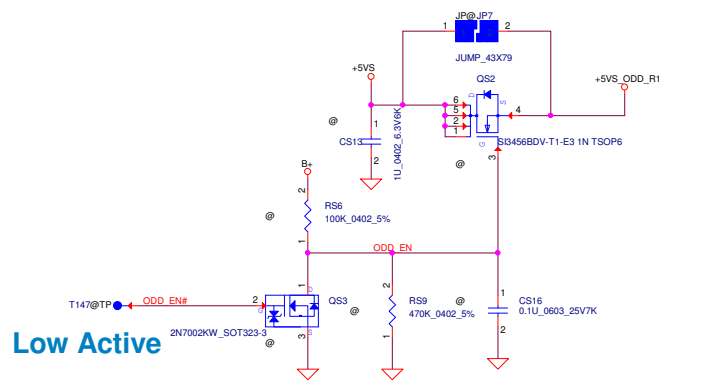


## SATA HDD Connector



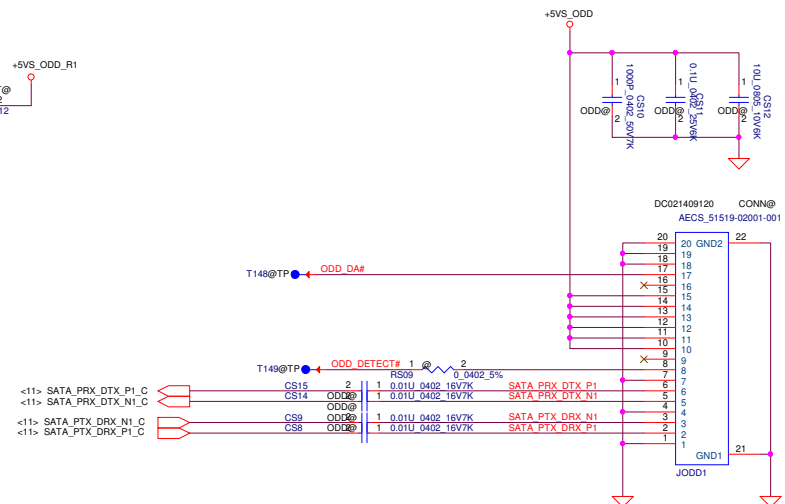
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## ODD Power Control



Low Active

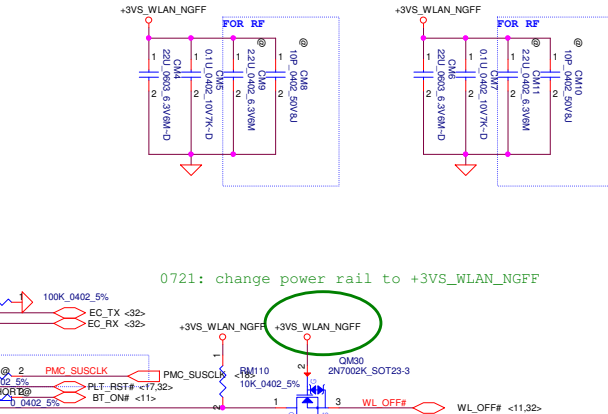
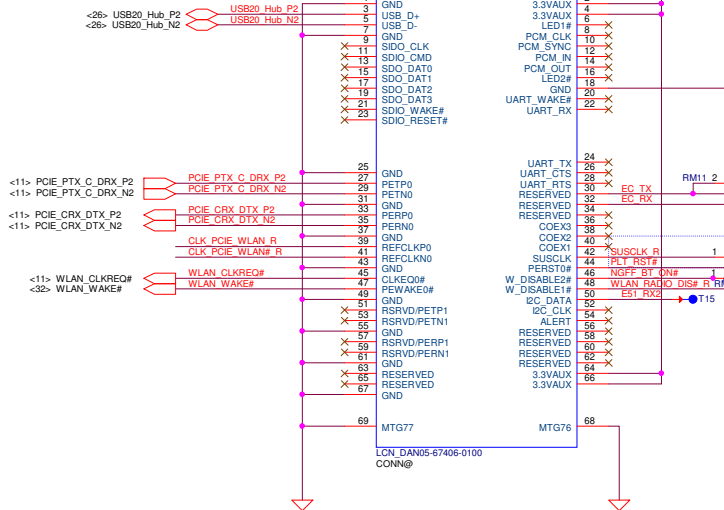
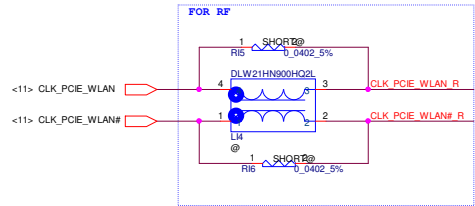
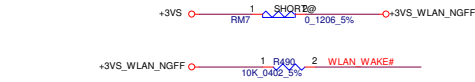
## SATA ODD Connector



Main Func = NGFF

closed to pin 2, 4

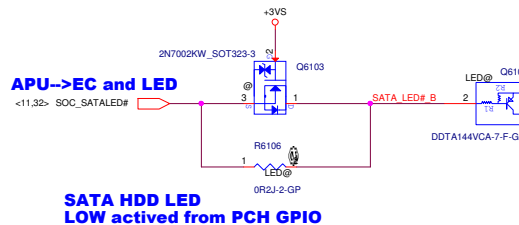
closed to pin 64, 66



0721: change power rail to +3VS\_WLAN\_NGFF

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### HDD LED



APU-->EC and LED

<11,32> SOC\_SATALED#

SATA HDD LED

LOW activated from PCH GPIO

Power / Battery LED

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

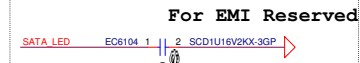
Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO

Low activated from KBC GPIO



For EMI Reserved

SATA LED

EC6104 1

SCD1U16V2KX3GP

2nd = 83.00110.070

3rd = 083.11204.0070

2nd = 83.00110.070

3rd = 083.11204.0070

2nd = 83.00110.070

3rd = 083.11204.0070

2nd = 83.00110.070

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2nd = 83.00110.070

3rd = 083.11204.0070

2nd = 83.00110.070

3rd = 083.11204.0070

2nd = 83.00110.070

3rd = 083.11204.0070

### Battery LED1 (YELLOW LED)

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

Battery LED1

### Battery LED2 (WHITE\_LED)

Battery LED2

Battery LED2

Battery LED2

Battery LED2

Battery LED2

Battery LED2

Battery LED2

Battery LED2

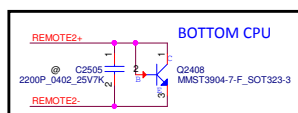
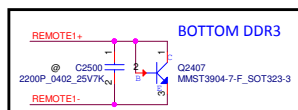
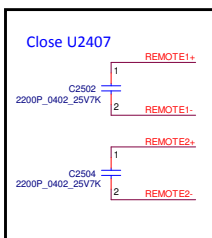
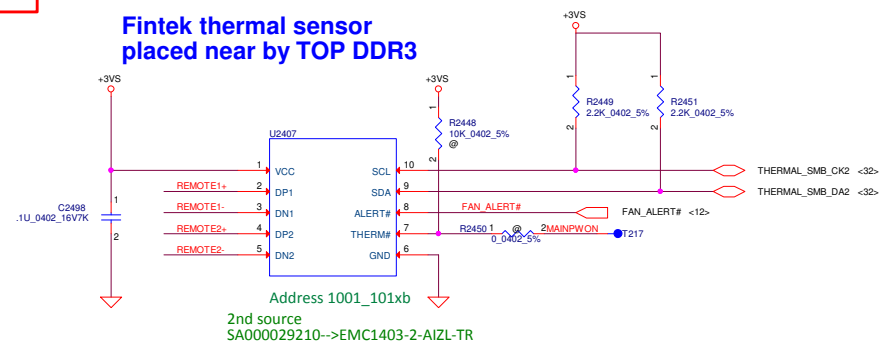
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Issued Date	2014/11/10	Deciphered Date	2015/11/25
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		Rev	1.0
		Date	Tuesday, June 16, 2015
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**Main Func = Thermal**

**Fintek thermal sensor  
placed near by TOP DDR3**

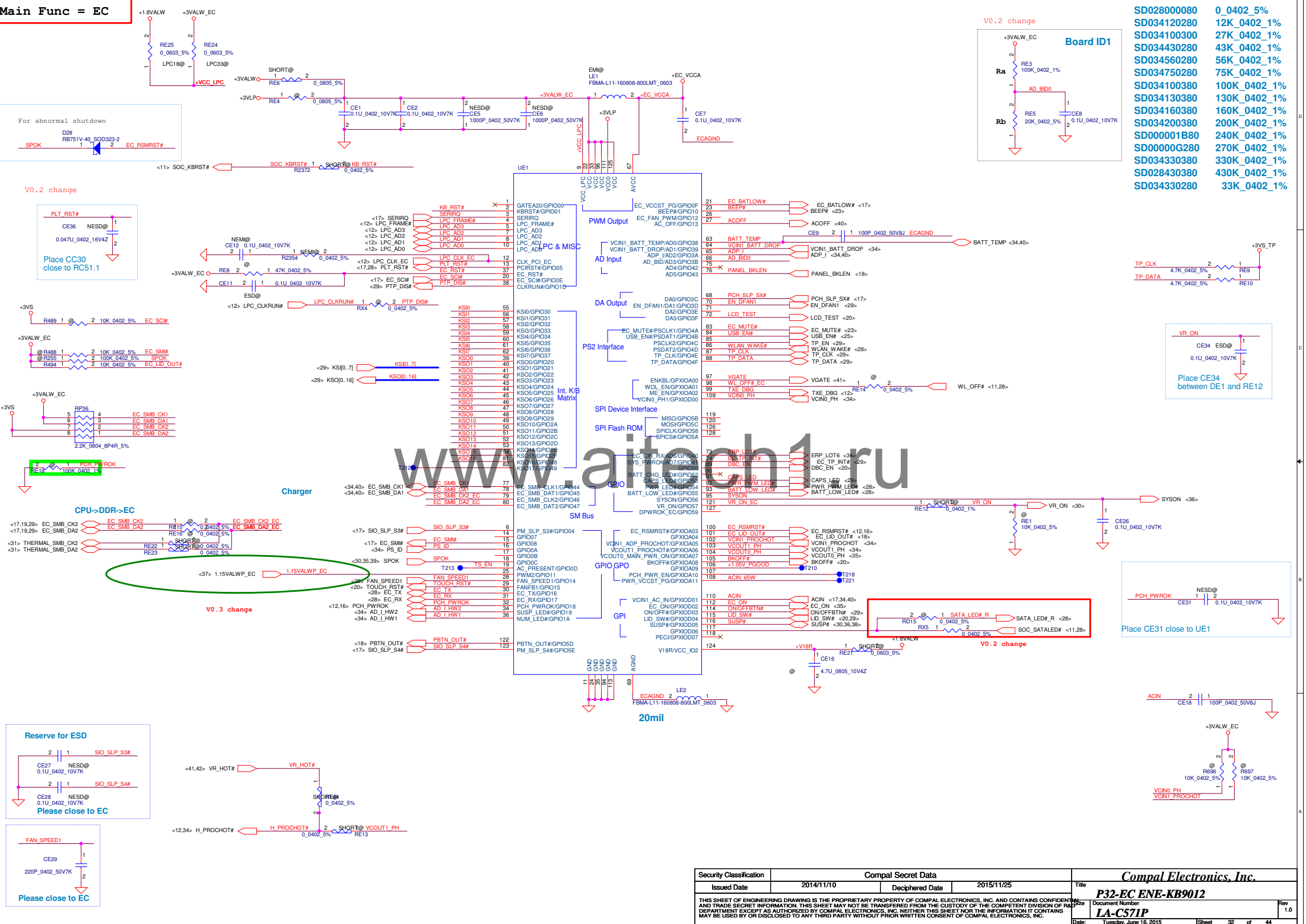


REMOTE1,2 (+/-) :  
Trace width/space:10/10 mil  
Trace length:<8"

[www.aitech1.ru](http://www.aitech1.ru)

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Date	Tuesday, June 16 2015	Sheet	31 of 44			

Main Func = EC

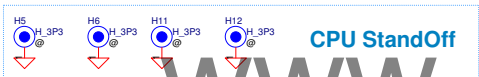
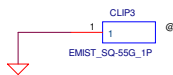
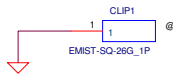
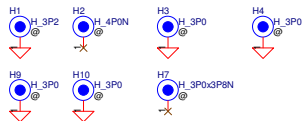


SD028000080	0_0402_5%
SD034120280	12K_0402_1%
SD034100300	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD000001B80	240K_0402_1%
SD00000G280	270K_0402_1%
SD034330380	330K_0402_1%
SD028430380	430K_0402_1%
SD034330280	33K_0402_1%

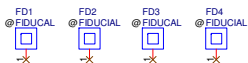


Main Func = Screw Hole

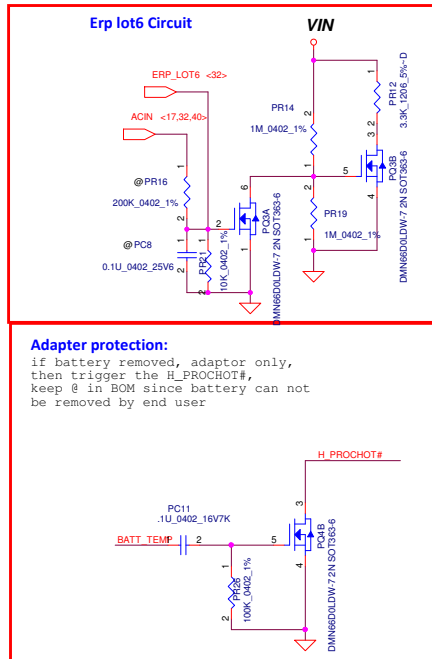
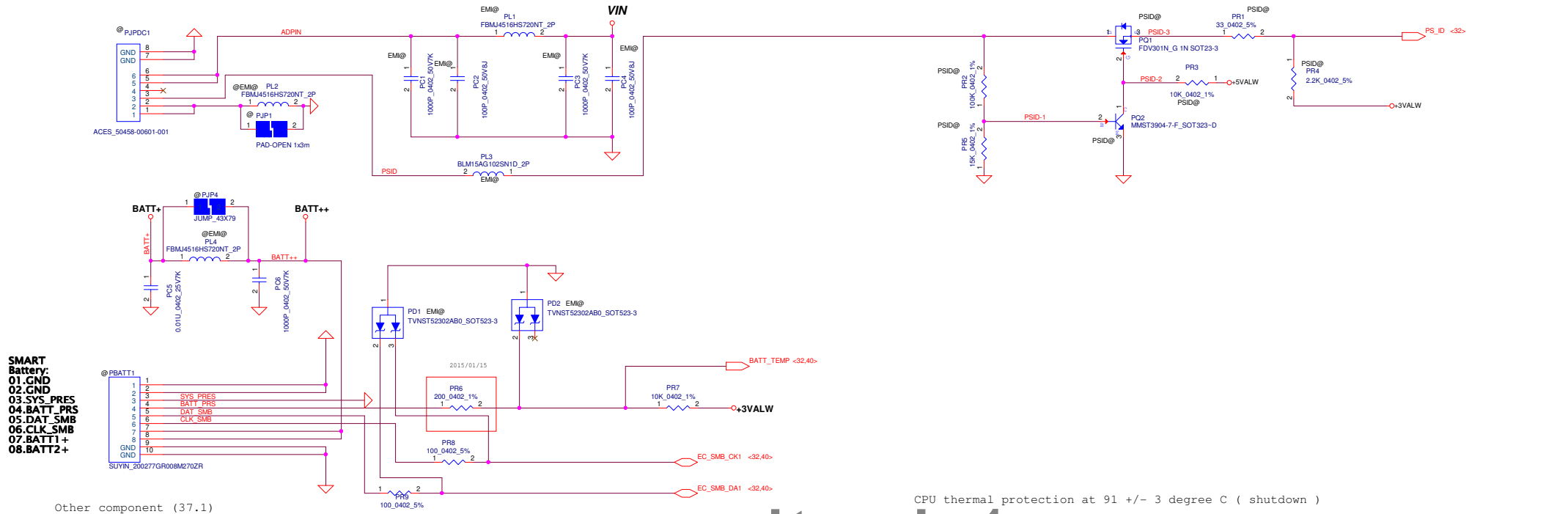
Screw Hole



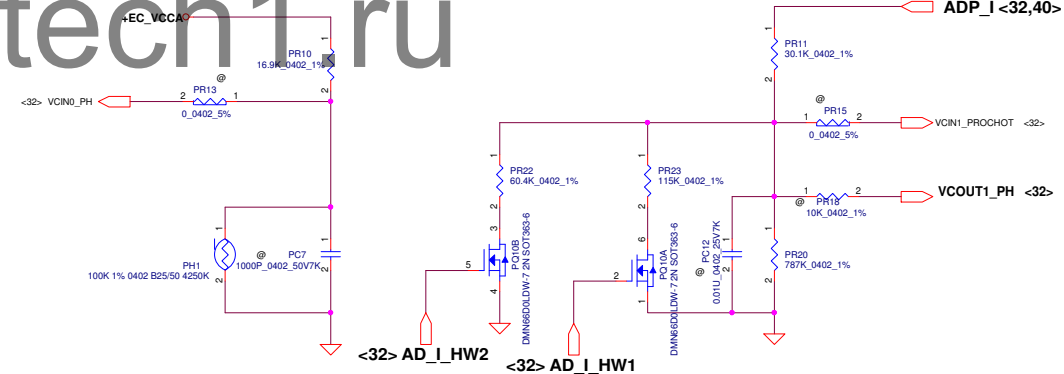
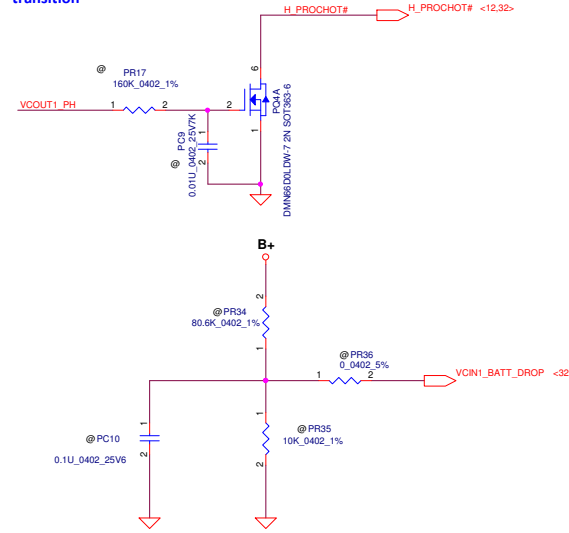
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				Document Number	
				LA-C571P	
Date:				Tuesday, June 16, 2015	
				ISheet	33 of 44



Delay adaptor OC\_H\_PROCHOT#  
 2ms while hybrid power  
 transition

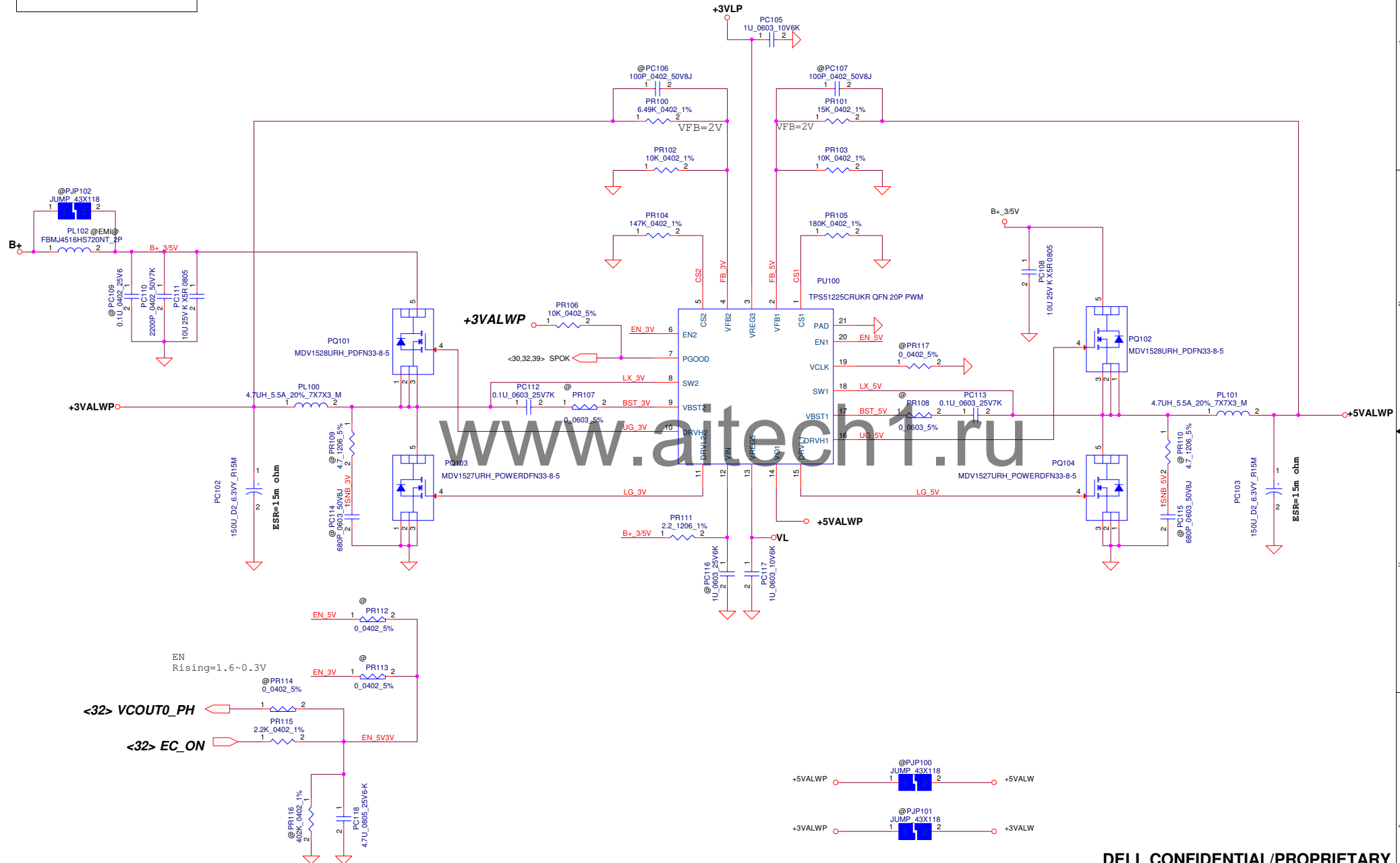


ADP\_I(with selector) to support "PWC" function.

H_PROCHOT#	AD_I_HW1	AD_I_HW2
35W	0	0
45W	1	0
55W	0	1
65W	1	1

3VALWP  
TDC 5.25A  
Peak Current 6.56A  
OCP current 8.53A

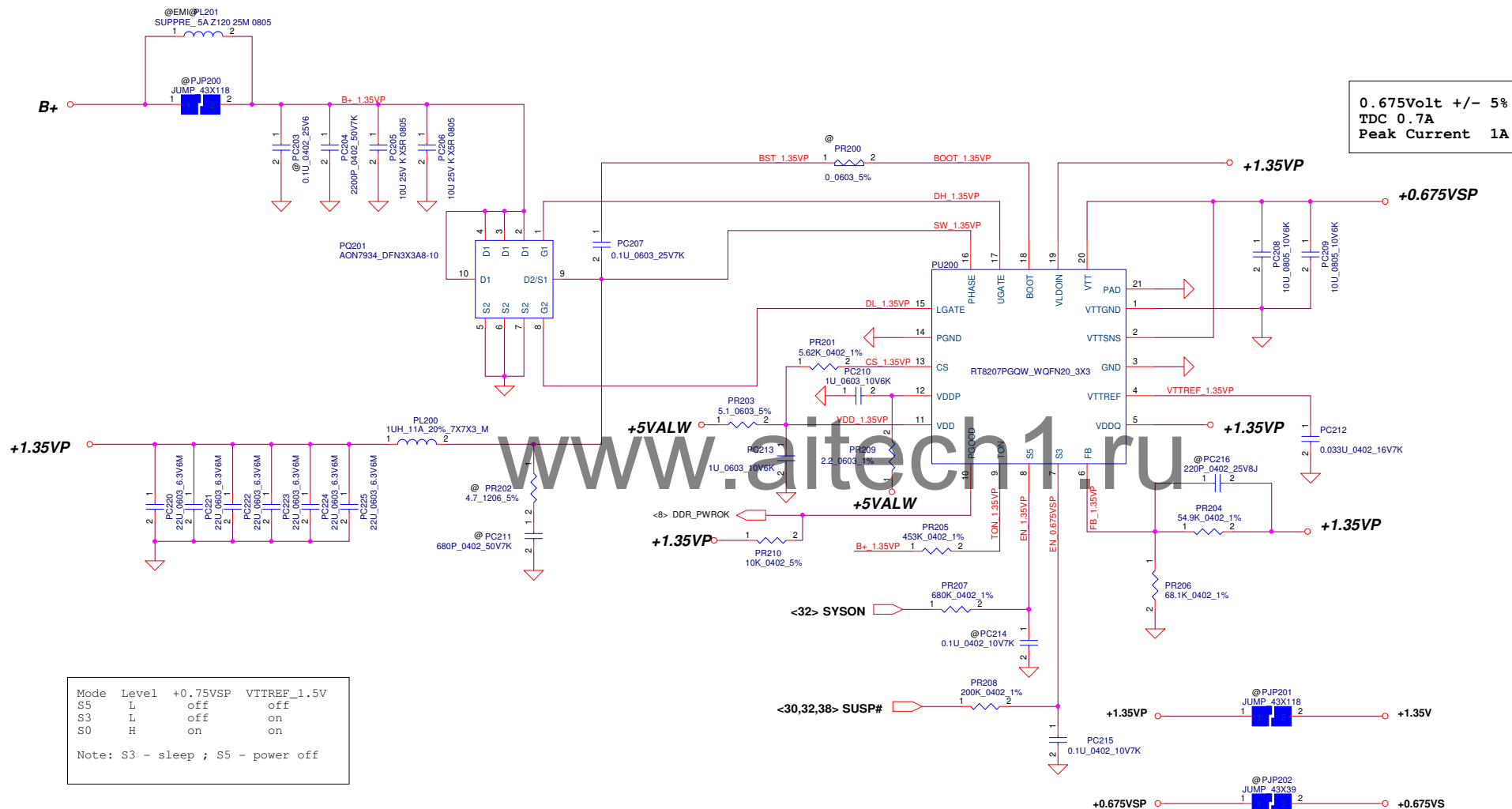
5VALWP  
TDC 5.3A  
Peak Current 6.62A  
OCP current 8.61A



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<p>Document Number <b>LA-B911P</b></p> <p>Date: Tuesday, June 16, 2015 Sheet 35 of 44</p>				

1.35VP  
TDC 3.6A  
Peak Current 4.5A  
OCP current 6A

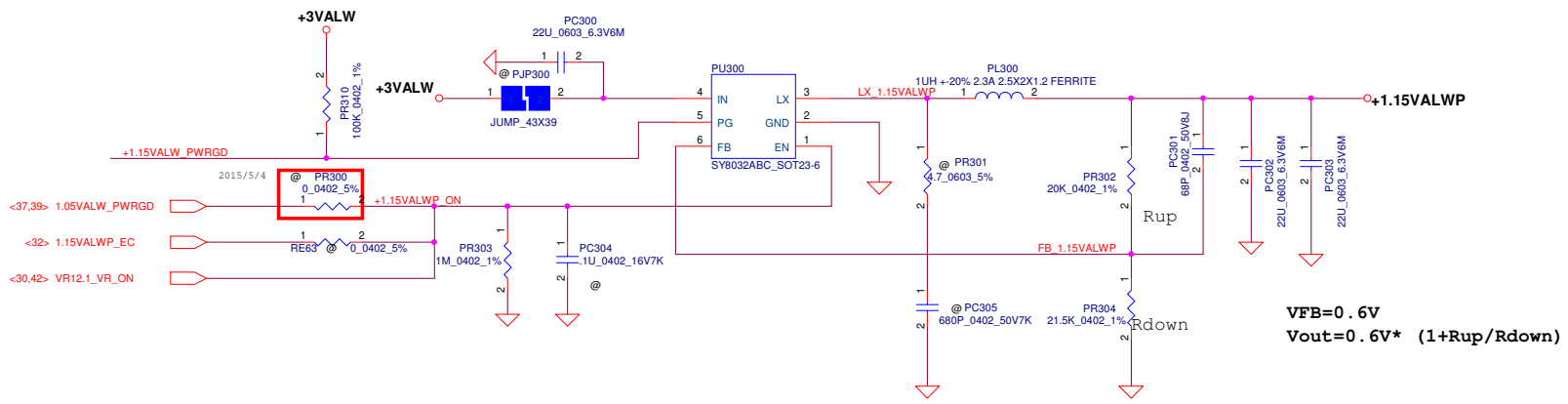


Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

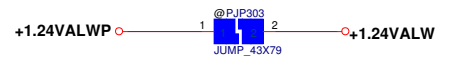
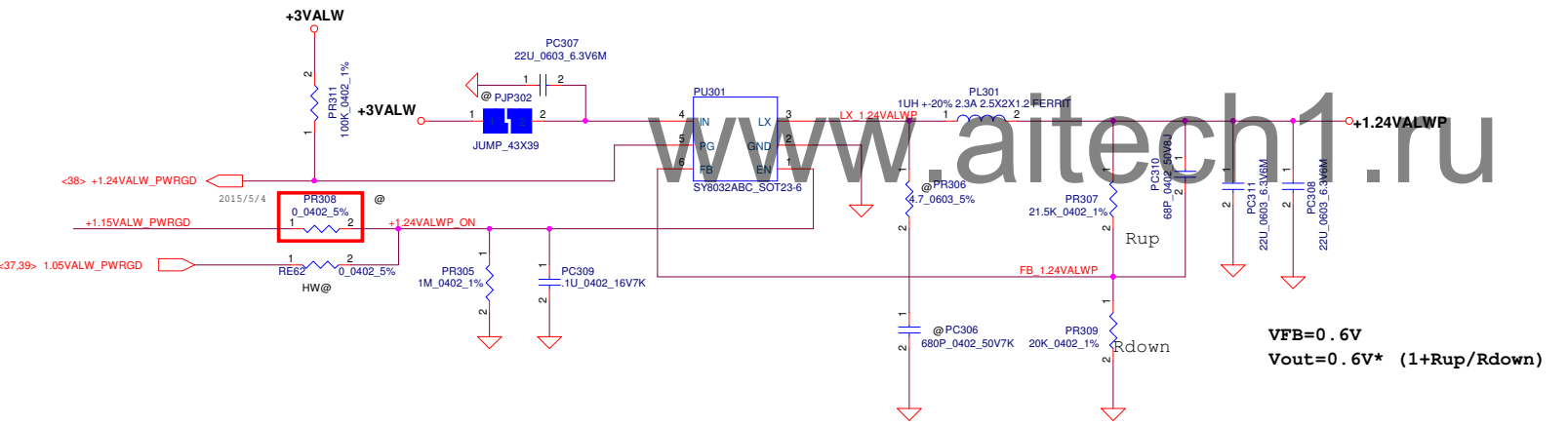
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**+1.15VALWP**  
TDC 0.64A  
Peak Current 0.8A  
OCP current 3.5A

$V_{FB} = 0.6V$   
 $V_{out} = 0.6V * (1 + R_{up}/R_{down})$

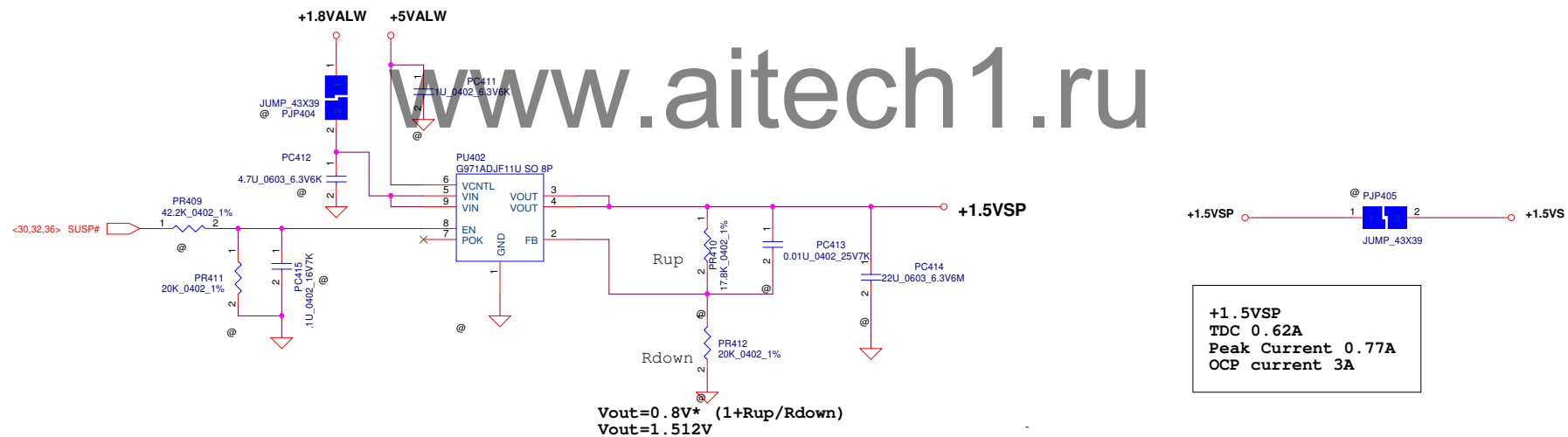
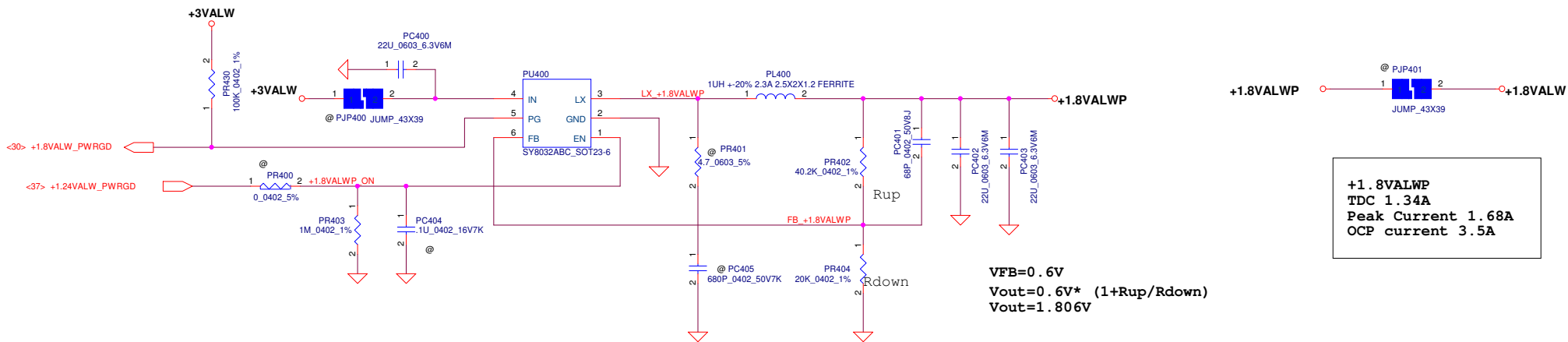


**+1.24VALWP**  
TDC 0.72A  
Peak Current 0.9A  
OCP current 3.5A

$V_{FB} = 0.6V$   
 $V_{out} = 0.6V * (1 + R_{up}/R_{down})$

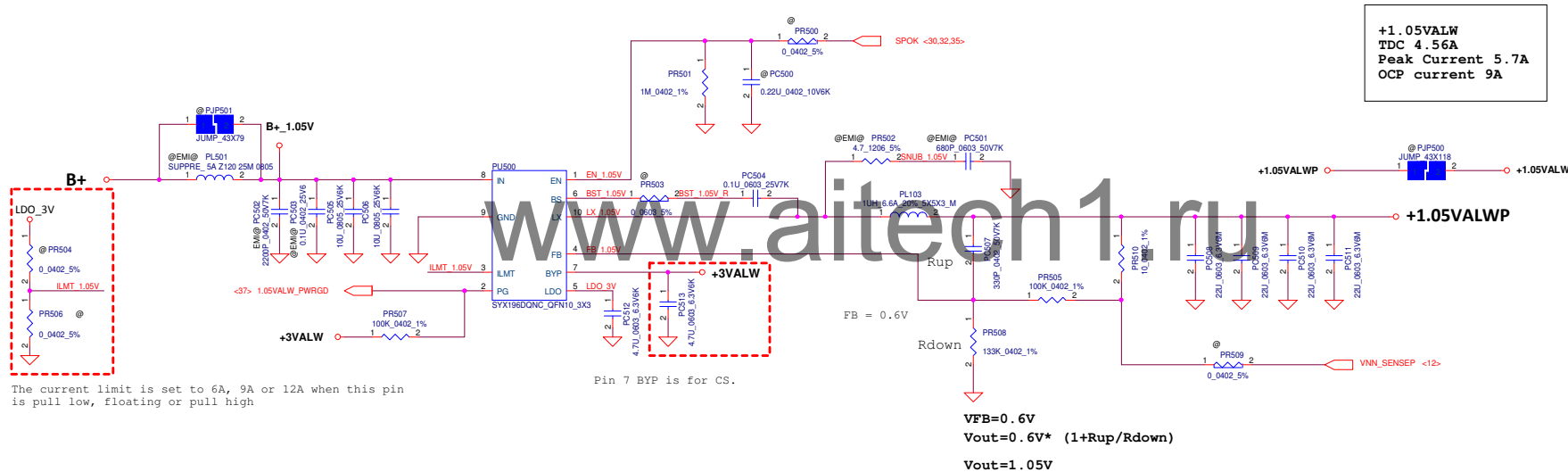
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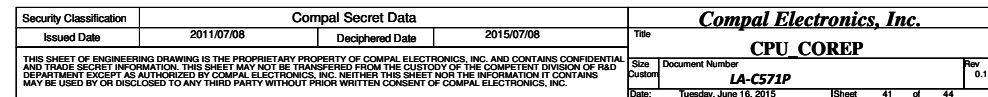
Security Classification		Compal Secret Data				Compal Electronics, Inc.			
Issued Date		2014/02/26		Deciphered Date		2015/02/25		Title	
								P38-PWR-1.8VALW/1.5VSP	
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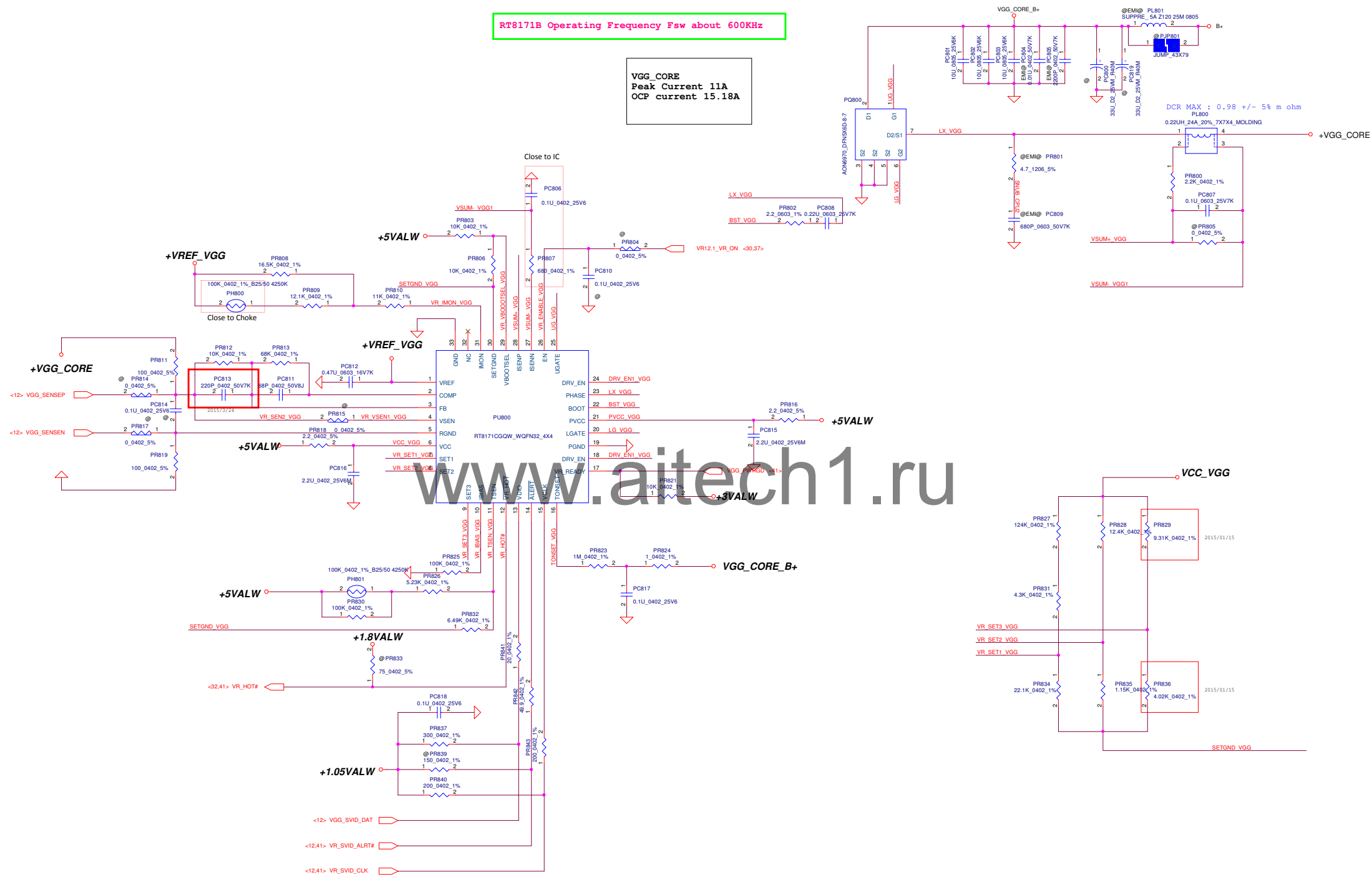


```
VCC_CORE
Peak Current 7.7A
OCP current 9.66A
```



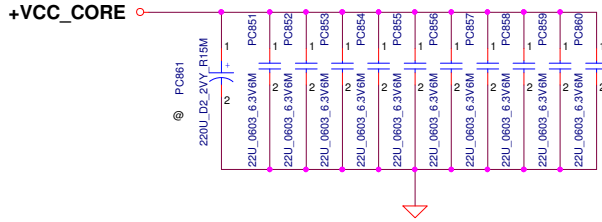
RT8171B Operating Frequency Fsw about 600KHz

```
VGG_CORE
Peak Current 11A
OCP current 15.18A
```

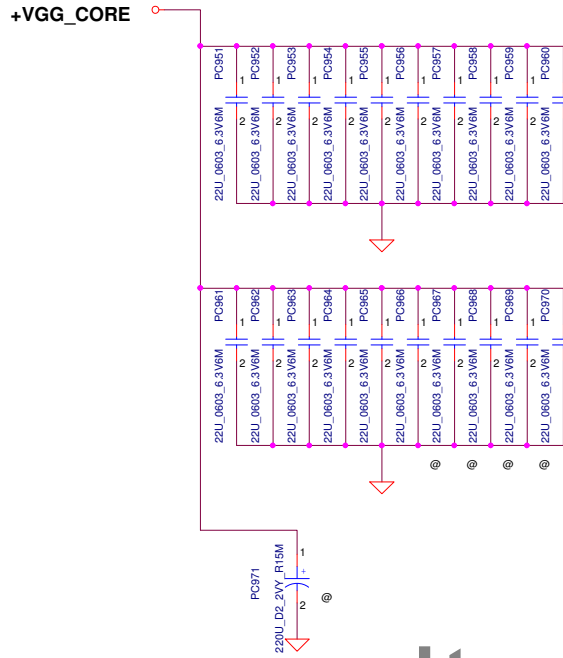


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				Date: Tuesday, June 16, 2015	Rev 0.1
				Sheet	42 of 44

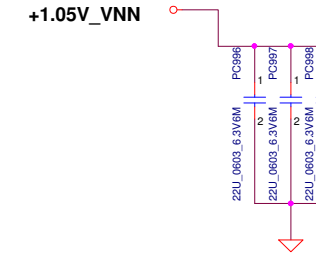
22U\_0603 \* 14 + reserved+220uF 15m ohm



22U\_0603 \* 16 +4 reserved+220uF 15m ohm

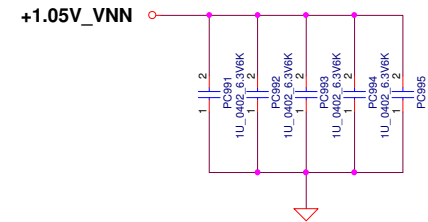
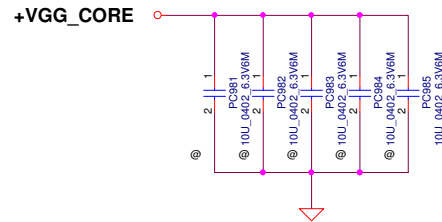
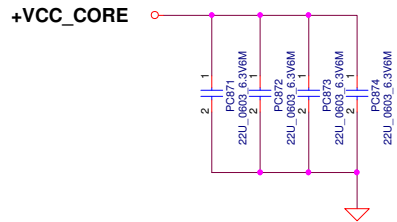


22U\_0603 \* 3



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Place on CPU Back Side.



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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1		For PS2/PS3 ripple			PR829 change 976 from to 9.31Kohm , PR836 change 412 from to 4.02K ohm	15/01/15	EVT
2		For PS2/PS3 ripple			PR829 change 39.2k from to 48.9Kohm , PR636 change 14k from to 17.4K ohm , PC612 change form 470pF to 270pF	15/01/15	EVT
3		Compal ESD team request			PR6 change 100ohm from to 200 ohm	15/01/15	EVT
4		For HW power sequency			PR300 change to reserve	4/05/15	DVT2
5		For HW power sequency			PR308 change to reserve	4/05/15	DVT2
5							
6							
7							

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				Custom	1.0
Date:				Sheet	44 of 44